COMP2121: Microprocessors and Interfacing

Course Introduction

http://www.cse.unsw.edu.au/~cs2121

Lecturer: Hui Wu

Term 2, 2019

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COMP2121 Administration (1/2)

Lecturer:

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Consultation: Friday: 2:00–5:00pm

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COMP2121 Administration (2/2)

Course Homepage: http://www.cse.unsw.edu.au/~cs2121 or https://webcms3.cse.unsw.edu.au/COMP2121/19T2/

Course homepage contains:

- Lecture slides
- Lab specifications
- Project
- Homework
- All material relating to the lab exercises
- Supplementary material
- Forum
- Announcements

Check it out frequently!

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Syllabus (1/2)

Main Topics:

- Instruction Set Architecture (ISA)
- AVR Assembly Language Programming
- Interrupts
- I/O Devices
- Parallel Input and Output
- Serial Communication
- Analog Input and Output
- Instruction Pipelining
- Caches

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Syllabus (2/2)

Laboratory exercises

- AVR assembly programming and I/O interfacing with AVR Studio and AVR board
- Weeks 2-10

Project

- One project, group work (2 students per group)
- Implement a monorail emulator using AVR board
- Due on Friday Week 11

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Lab Format

- In a group of two students
- Choose your partner in the first lab (Week 2). You will get a group account from a tutor.
- After you finish a task, ask a tutor to mark it. The tutor will ask you to explain how your code works, and some questions.
- Ask a tutor to help when you have questions
  - You cannot ask a lab tutor to give you the solution to a task.

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Lab Preparation

° You can finish the laboratory exercises in the allocated time only if you do the preparation before hand

° Before attending each lab, you need to prepare for it by:

- carefully reading the lab related material, and
- writing most of your programs and simulating them at home

° Leaving things to the last minute or walking into the lab without preparation may make you fail this course

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Laboratory Structure & Specifications

- 5 labs in total
  - ❑ Each lab consists of several tasks
  - ❑ Use AVR Studio to do Labs 1&2
  - ❑ Collect an AVR board in Week 5 and use it in Labs 3-5
    - ➢ Keep your board in good condition
- Lab specifications will be available on the course homepage one week before each lab starts

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Homework

- Homework will be released every week
- Not assessed
- You need to work out solutions in order to understand the course material
- My solutions will be released one week later
- Homework is designed to help you understand the course material and prepare for the exam.

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Course Assessment Scheme

- Labs: 25%
- Project 15%
- Final exam: 60%
  - 2 hours, closed book, written exam

To pass this course, you MUST get at least 50% of the full marks in the labs, return the lab kits, and achieve at least 40/100 in the final exam and 50/100 in the final result.

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Microprocessors & microcontrollers are everywhere in our lives.

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Why AVR?

- RISC architecture with load-store memory accesses
- two-stage instruction pipelining
- Internal program memory (FLASH) and data memory (SRAM)
- Wide variety of on-chip peripherals (digital I/O, ADC, EEPROM, UART, pulse width modulator (PWM) etc)

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