Easter Homework

Comparing the Instruction Set Architectures of ARM and AVR

In this homework, you will learn the ISA of another RISC microprocessor, ARM, and compare it with that of AVR. As you are aware by now, an ISA consists of four components: memory models; registers; instructions; and, data types. Explore each component. **You should focus on 32-bit ARMv7 cores that target similar embedded markets to AVR (e.g. Cortex-M3).** The following sections will help.

1. Overview

In this section, focus on the overview of ARM microprocessors. Examine the salient features of the ARM architecture. Examples include pipelining, architecture, conditional execution, hardware support for power saving, caching and hardware support for floating point operations.

2. Memory models

How many memory spaces are there in ARM? What is the purpose of each memory space? What is the maximum memory size for each memory space?

3. Registers

What types of registers are available in the ARM architecture? How do the ARM general purpose registers compare with the AVR registers?

What is the ARM equivalent of AVR's SREG? How does it differ from AVR?

Compare ARM's interrupt system with AVR's.

4. Instruction Set

Examine the two ARM instruction encoding schemes and compare with AVR.

Learn the function and operation of ARM's predicated instructions.

Compare the instructions used for stack operations in ARM and AVR processors.

Learn about how ARM processors access I/O registers and compare with AVR.

What addressing modes are available with ARM load/store instructions? How are these different from the addressing modes available in AVR?

5. Data types

What data types can be natively represented by ARM's registers? Can the ARM instruction set be used to operate on 64-bit integers? What instructions would be used to implement a 64-bit signed integer addition?

7. Conclusion

After comparing the ISA of ARM and AVR, you should know what kind of embedded systems will benefit from AVR and ARM.

Understand a) the main advantages and disadvantages of each architecture; and b) What applications each architecture is best suited to.