COMP2121: Microprocessors and Interfacing

Analog Input and Output

http://www.cse.unsw.edu.au/~cs2121

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Overview

- Analog-to-Digital (A/D) Conversion
- Shannon's Theorem
- A/D Converter Types
- A/D Converter Specifications
- Digital-to-Analog Conversion
- D/A Converter Types
- D/A Converter Specifications
- Pulse-Width-Modulated (PWM) Analog Output
- PWM Wave Generation in AVR

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Analog Signals versus Digital Signals

Analog signals:

- Continuous in both time and amplitude.
- Noise sensitive.
- Cannot be manipulated by the computer.

Digital signals:

- Discrete in both time and amplitude.
- Generally free from noise.
- Can be manipulated by the computer.
- cannot exactly represent or reconstruct analog signals.

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Data Acquisition and Conversion (1/2)

Procedure of data acquisition and conversion:

1. A transducer converts physical processes to electrical signals, either voltages or currents.
2. Signal conditioner performs the following tasks:
   a. Isolation and buffering: The input to the A/D may need to be protected from dangerous voltages such as static charges or reverse polarity voltages.
   b. Amplification: Rarely does the transducer produce the voltage or current needed by the A/D. The amplifier is designed so that the full-scale signal from the analog results in a full-scale signal to the A/D.
   c. Bandwidth limiting: The signal conditioning provides a low-pass filter to limit the range of frequencies that can be digitized.

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Data Acquisition and Conversion (2/2)

3 In applications where several analog inputs must be digitized, an analog multiplexer follows the signal conditioning. It allows multiple analog inputs, each with its own signal conditioning for different transducers.

4 The sample-and-hold circuit samples the signal and holds it steady while the A/D converts it.

5 The A/D converter converts the sampled signal to digital values.

6 The three state gates hold the digital values generated by the A/D converter.

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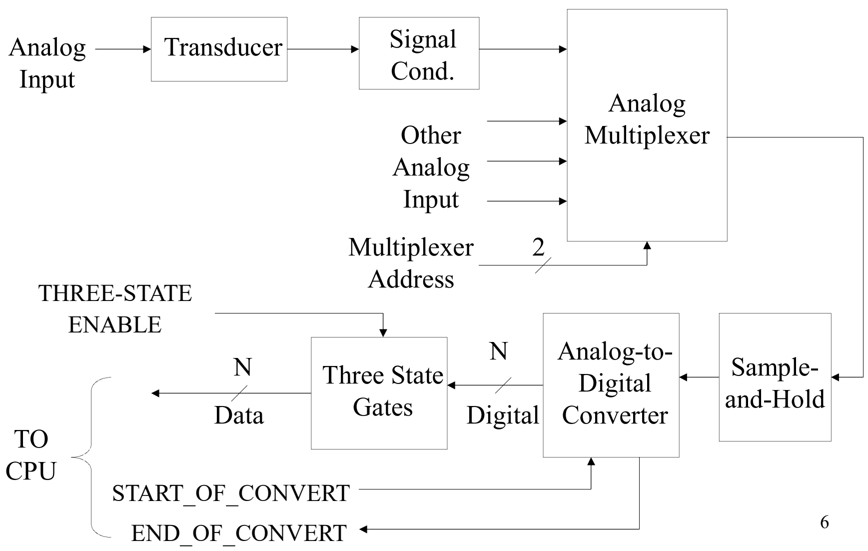
Data Acquisition System



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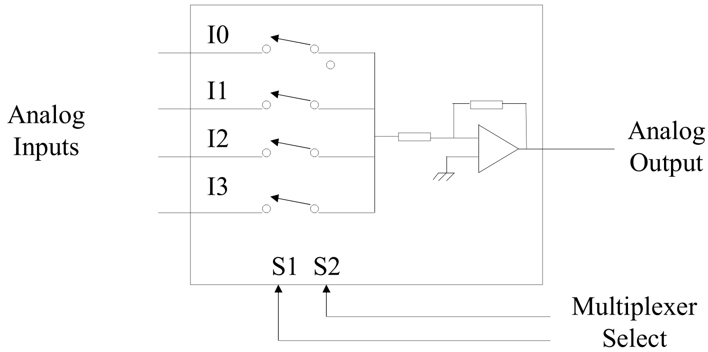
Analog Signal Multiplexer



- The multiplexer is selected by the CPU generating an address on the multiplexer select lines.

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Shannon's Sampling Theorem and Aliasing (1/6)

Claude Shannon's Theorem:

- When a signal, $f(t) = X \sin(2\pi f_{sig} t)$, is to be sampled (digitized), the minimum sampling frequency must be twice the signal frequency.

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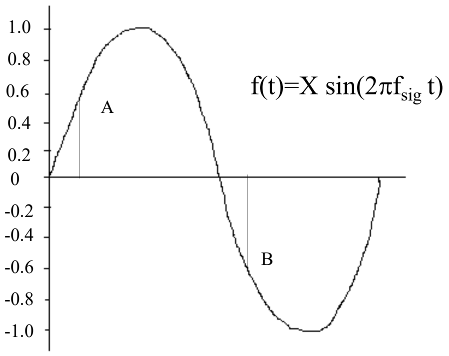
Shannon's Sampling Theorem and Aliasing (2/6)



Sinusoidal waveform sampled at twice the signal frequency.

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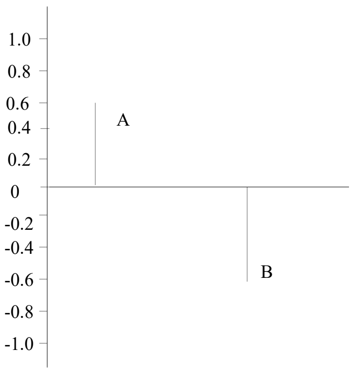
Shannon's Sampling Theorem and Aliasing (3/6)



Sampled waveform.

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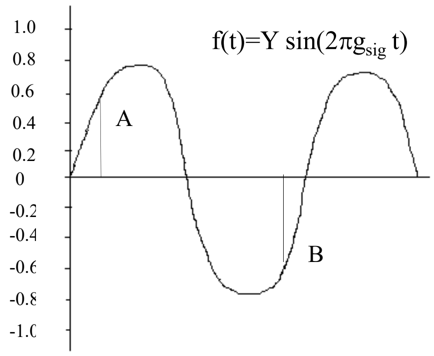
Shannon's Sampling Theorem and Aliasing (4/6)



Undersampled waveform.

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Shannon's Sampling Theorem and Aliasing (5/6)

- To preserve the full information in the signal, it is necessary to sample at twice the maximum frequency of the signal. This is known as the Nyquist rate.
- A signal can be exactly reproduced if it is sampled at a frequency F, where F is greater than twice the maximum frequency in the signal.
- If the sampling frequency is less than Nyquist rate, the waveform is said to be undersampled.

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Shannon’s Sampling Theorem and Aliasing (6/6)

- Undersampled signal, when converted back into a continuous signal, will exhibit a phenomenon called ***aliasing***.
  - ❑ Aliasing is the presence of unwanted components in the reconstructed signal. These components were not present when the original signal was sampled. In addition, some of the frequencies in the original signal may be lost in the reconstructed signal.

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A/D Converter Types

- Successive approximation A/D.
- Tracking A/D converter.
- Dual-slope A/D converter.
- Parallel A/D converter.
- Two-stage parallel A/D converter.

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Successive Approximation A/D Converter (1/2)

- Each bit in the successive approximation register is tested, starting at the most significant bit and working toward the least significant bit.
- As each bit is set, the output of the D/A converter is compared with the input.
- If the D/A output is lower than the input signal, the bit remains set and the next bit is tried.
- Bits that make the D/A output higher than the analog input are reset.
- N bit-times are required to set and test each bit in the successive approximation register.

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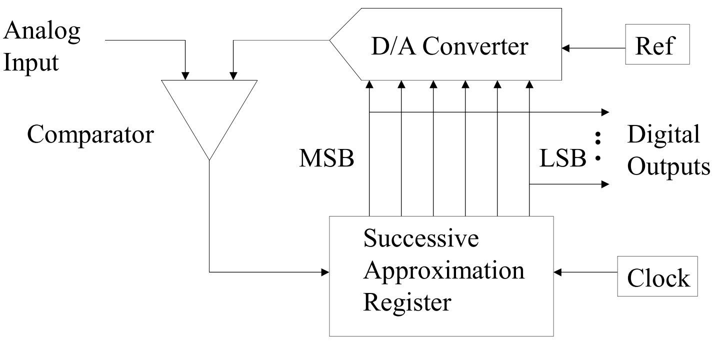
Successive Approximation A/D Converter (2/2)



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Tracking A/D Converter (1/2)

- Close cousin of the successive approximation converter.
- Has a up/down counter controlled by the comparator.
- If the input signal is higher or lower than the output of the D/A converter, the counter counts up or down, respectively.
- May quickly converge to the correct digital value when the signal is not changing rapidly.
- May have to count through its full range before reaching the final stage if large, rapid, input changes are seen.

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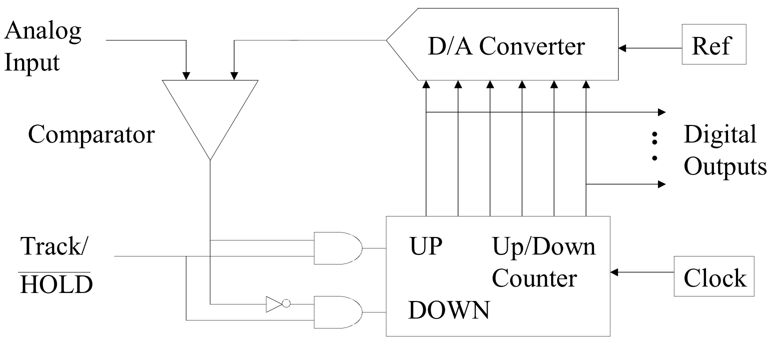
Tracking A/D Converter (2/2)



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Dual Slope A/D Converter (1/3)

- Also called integrating A/D converter.
- Integrates the input signal for a fixed time, T_1, with higher input signals integrating to higher values.
- During the second period, T_2, the switch is changed to the minus reference voltage and the integrator discharges to zero at a constant rate. The time it takes to discharge, T_2, gives digital value.
- It is remarkably efficient at recovering signals from periodic noise.

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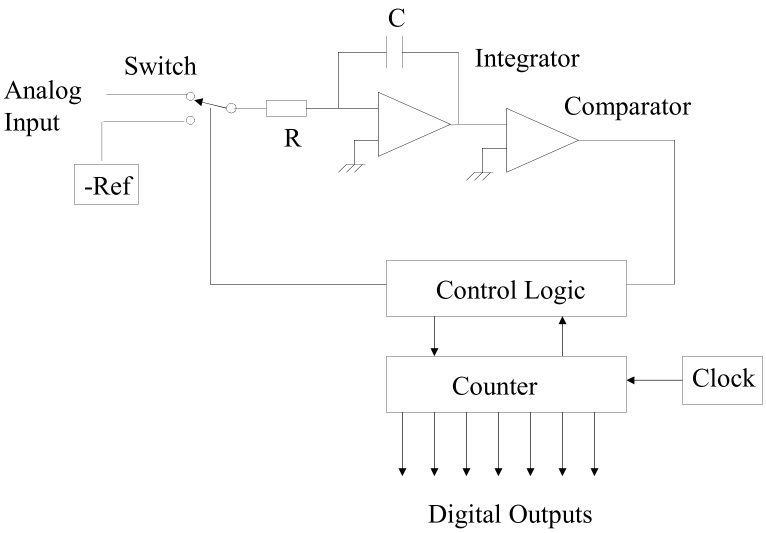
Dual Slope A/D Converter (2/3)



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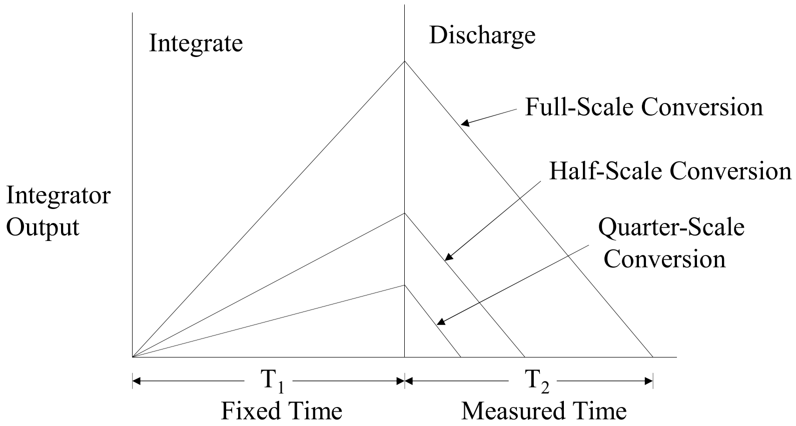
Dual Slope A/D Converter (3/3)



Integrator output for dual-slope A/D

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Parallel A/D Converter (1/2)

- An array of 2^N-1 comparators and produces an output code in the propagation time of the comparators and the output decoder.
- Fast but more costly in comparison to other designs.
- Also called flash A/D converter.

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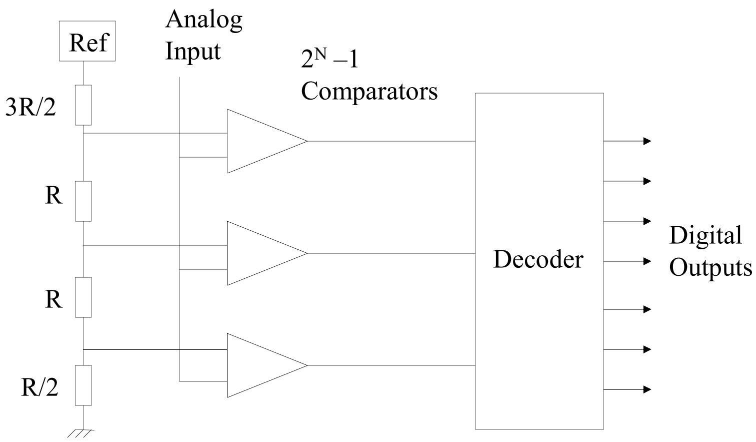
Parallel A/D Converter (2/2)



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Two-Stage Parallel A/D Converter (1/2)

- The input signal is converted in two pieces.
  - ❑ First, a coarse estimate is found by the first parallel A/D converter. This digital value is sent to the D/A and summer, where it is subtracted from original signal.
  - ❑ The difference is converted by the second parallel converter and the result combined with the first A/D to give the digitized value.
- It has nearly the performance of the parallel converter but without the complexity of $2^N - 1$ comparators.
- It offers high resolution and high-speed conversion for applications like video signal processing.

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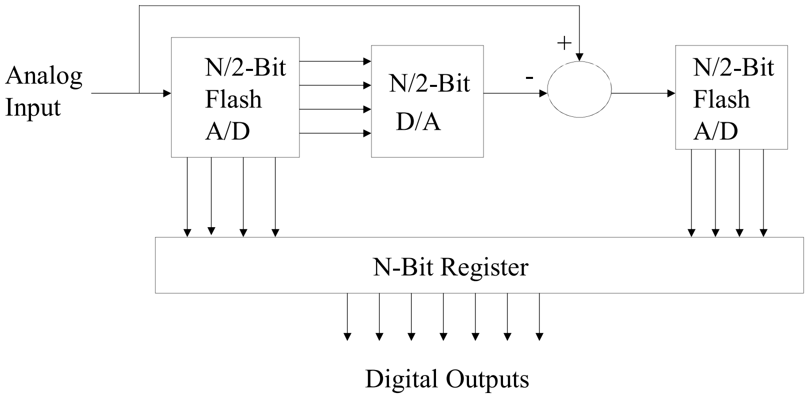
Two-Stage Parallel A/D Converter (2/2)



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A/D Converter Specifications (1/7)

- Conversion time.
  - ❑ The time required to complete a conversion of the input signal.
  - ❑ Establishes the upper signal frequency limit that can be sampled without aliasing.

    f_{MAX}=1/(2*conversion time) (1)
- Resolution.
  - ❑ The number of bits in the converter gives the resolution and thus the smallest analog input signal for which the converter will produce a digital code.
  - ❑ It may be given in terms of the full-scale input signal:

    Resolution=full-scale signal/2^n (2)
  - ❑ It is often given as the number of bits, n, or stated as one part in 2^n.
  - ❑ Sometimes it is given as a percent of maximum.

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A/D Converter Specifications (2/7)

- Accuracy.
  - ❑ Relates to the smallest signal (or noise) to the measured signal.
  - ❑ Given as a percent and describes how close the measurement is to the actual value.

  The signal is accurate to within 100% * $V_{RESOLUTION}/V_{SIGNAL}$ (3)
- Linearity.
  - ❑ The deviation in output codes from a straight line drawn through zero and full-scale.
  - ❑ The best that can be achieved is ± ½ of the least significant bit (± ½ LSB).

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A/D Converter Specifications (3/7)

- Missing codes.
  - ❑ A missing code could be caused by an internal error, especially by the A/D converter in a successive approximation converter.
- Aperture time.
  - ❑ The time that the A/D converter is "looking" at the input signal.
  - ❑ It is usually equal to the conversion time.

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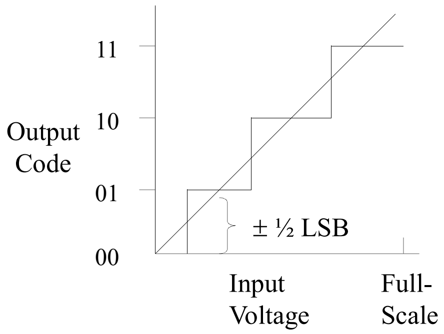
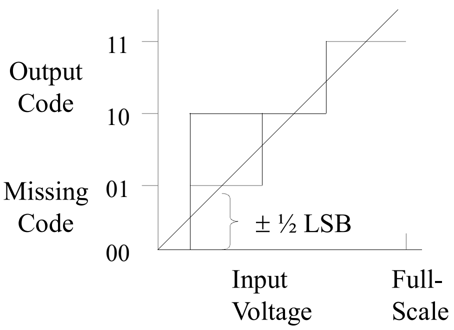
A/D Converter Specifications (4/7)



A/D linearity



A/D missing codes

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A/D Converter Specifications (5/7)

Example 1 An A/D converter has a conversion time of 100 μs. What is the maximum frequency that can be converted without aliasing?

Solution:

The maximum sampling frequency is the reciprocal of the the conversion time=10 kHz.

The maximum signal frequency that can be converted is 5 kHz.

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A/D Converter Specifications (6/7)

Example 2 An 8-bit A/D converter is to digitize a five-volt, full scale signal. What is the resolution?

Solution:

The resolution is 5/256=19.5 mV. Another way of stating the resolution is 1 part in 256 or 0.4% of the full-scale value.

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A/D Converter Specifications (7/7)

Example 3 An 8-bit A/D converter is to digitize a five-volt, full-scale signal. What is the accuracy with which the A/D converter can digitize the following signals?

50 mV, 1 V, 2.5 V, 4.9 V

Solution:

The resolution is 5 V/256=19.5 mV. The measurement will be accurate to within the following:

50 mV	(19.5 mV/50 mV) = 39%
1 V	(19.5 mV/1 V) = 1.9%
2.5 V	(19.5 mV/2.5 V) = 0.8%
4.9 V	(19.5 mV/4.9 V) = 0.4%

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A/D Errors (1/4)

Three sources of errors in A/D conversion:

- Noise.
  - All signals have noise.
  - Need to reduce noise or choose the converter resolution appropriately to control the peak-to-peak noise.
- Aliasing.
  - The errors due to aliasing is difficult to quantify.
  - They depend on the relative amplitude of the signals at frequencies below and above the Nyquist frequency.
  - The system design should include a low-pass filter to attenuate frequencies above the Nyquist frequency.

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A/D Errors (2/4)

- Aperture.
  - A significant error in a digitizing system is due to signal variation during the aperture time.
  - A good design will attempt to have the uncertainty, ΔV, be less than one least significant bit.
  - A design equation for the aperture time, t_{AP}, in terms of the maximum signal frequency, f_{MAX}, and the number of bits in the A/D converter is

$$t_{AP}=1/(2\,\pi\, f_{MAX}\, 2^{n}) \qquad (4)$$

  - The aperture time needed to reduce the error to ±1/2 LSB is surprisingly short.

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A/D Errors (3/4)

Example 4 A 1 kHz sinusoidal signal is to be digitized to eight bits. Find the maximum conversion time that can be used and still avoid aliasing and aperture time so that the aperture error is less than ± ½ LSB.

Solution: There must be at least two samples per period; so the maximum conversion time is 0.5 ms. The aperture time is given by Equation 4 and is

$$t_{AP} = 1/(2\pi * 10^3 * 256) = 0.62\ \mu s$$

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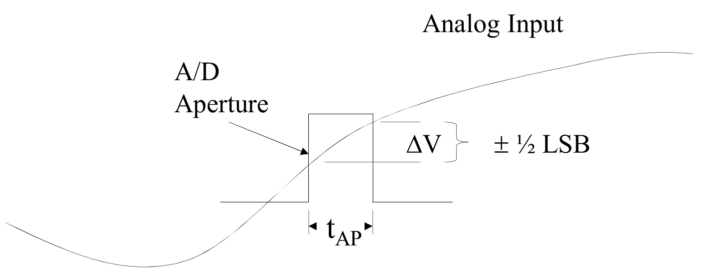
A/D Errors (4/4)



Aperture time error

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Sample-and-Hold (1/2)

- The sample-and-hold (S/H) circuit can achieve the short aperture time while allowing a less expensive converter to satisfy the conversion time.
- It is a high-quality capacitor and a high-speed semiconductor switch.
- The sample command closes the switch for a very short time, and the capacitor charges or discharges to the input voltage.
- When the switch is open, the voltage is held for the A/D during its conversion time.

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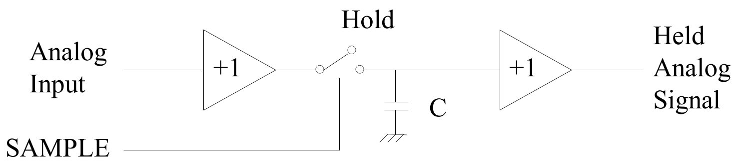
Sample-and-Hold (2/2)



Sample-and-hold circuit

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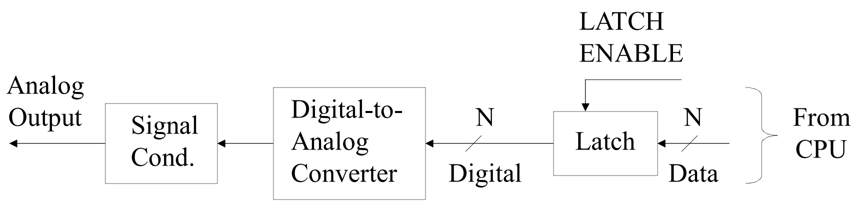
Digital-to-Analog Converter (1/2)



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Digital-to-Analog Converter (2/2)

- A parallel output interface connects the D/A to the CPU.
- The latches may be part of the D/A converter or the output interface.
- The analog output signal from the D/A is quantized.
- A signal conditioning block may be used as a filter to smooth the quantized nature of the output.
  - The signal conditioning block also provide isolation, buffering and voltage amplification if needed.

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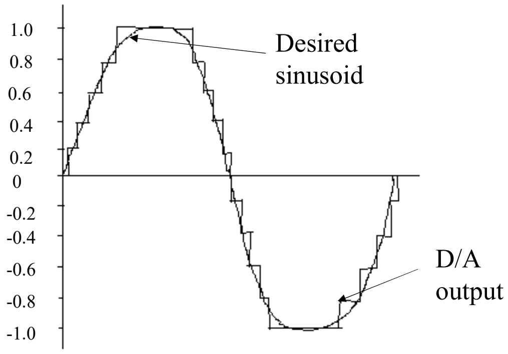
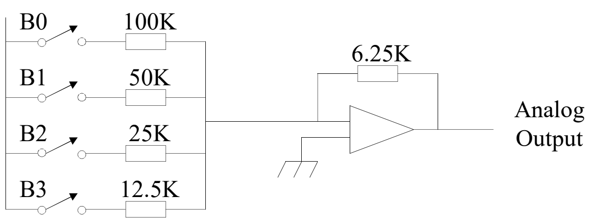
Quantized D/A Output



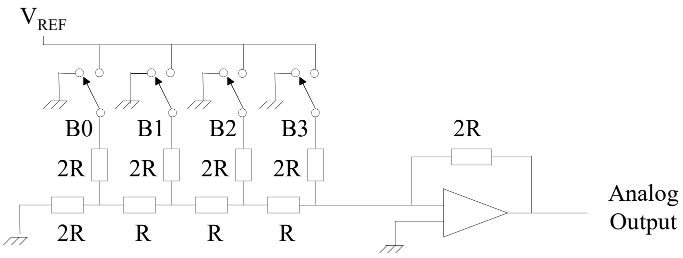
D/A Converter Types (1/3)

- Binary-weighted register D/A.
  - ❑ As the switches for the bits are closed, a weighted current is supplied to the summing junction of the amplifier.
  - ❑ For high-resolution D/A converters, the binary-weighted type must have a wide range of resistors. This may lead to temperature stability and switching problems.



D/A Converter Types (2/3)

- R-2R Ladder D/A.
  - ❑ As the switches are changed from the grounded to the reference position, a binary-weighted current current is supplied to the summing junction.
  - ❑ For high-resolution D/A converters, a wide range of resistors are not required. However, single-pole double throw switches are.



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D/A Converter Types (3/3)

- Multiplying D/A.
  - ❑ The R-2R ladder D/A can be used as a multiplying D/A by using reference voltage as an input. The reference voltage can vary over the maximum voltage range of the amplifier and is multiplied by the digital code.

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D/A Converter Specifications (1/2)

- Resolution and linearity.
  - ❑ The resolution is determined by the number of bits and is given as the output voltage corresponding to the smaller digital step, i.e. 1 LSB.
  - ❑ The linearity show how closely the output voltage follows a straight line drawn through zero and full-scale.
- Settling Time.
  - ❑ The time taken for the output voltage to settle to within a specified error band, usually ± ½ LSB.

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D/A Converter Specifications (2/2)

- Glitches.
  - ❑ A glitch is caused by asymmetrical switching in the D/A switches. If a switch changes from a one to a zero faster than from a zero to a one, a glitch may occur.
  - ❑ Consider changing the output code of a 8-bit D/A from 10000000 to 01111111. These codes are adjacent, and we expect the output to go from one-half full-scale to one resolution value less than that. However, if the switches can switch faster from a one to a zero, the output code will go through a transitory state sequence 10000000 to 00000000 to 01111111. This results in a short but sometimes noticeable glitch in the output signal. Glitches are especially noticeable in video displays.
  - ❑ D/A converter glitch can be eliminated by using a sample-and-hold. The S/H is strobed to sample the data after the glitch has occurred and after the D/A settling time.

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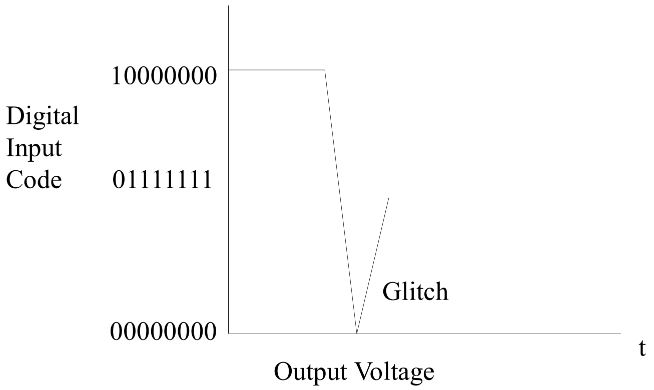
D/A Output Glitch



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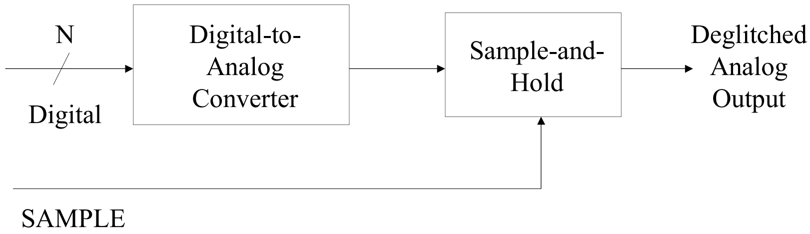
Deglitched D/A



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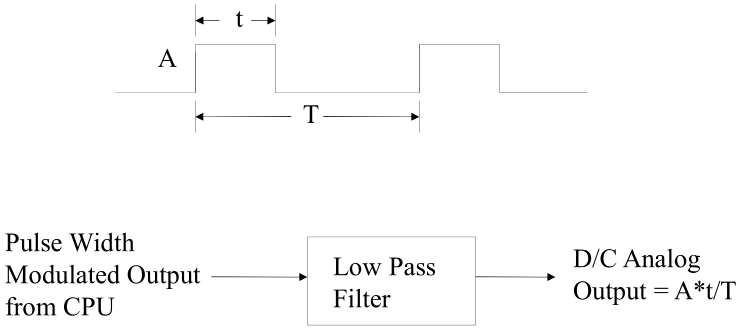
PWM Analog Output (1/5)

- PWM (Pulse Width Modulation) is a way of digitally encoding analog signal levels. Through the use of high-resolution counters, the *duty cycle* (pulse width/period) of a square wave is modulated to encode a specific analog signal level.
- The PWM signal is still digital because, at any given instant of time, the full DC supply is either fully on or fully off. The voltage or current source is supplied to the analog load by means of a repeating series of on and off pulses. Given a sufficient bandwidth, any analog value can be encoded with PWM.

PWM Analog Output (2/5)

- PWM is a powerful technique for controlling analog circuits with a processor's digital outputs.
- It is employed in a wide variety of applications, ranging from measurement and communications to motor speed control.

PWM Analog Output (3/5)



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PWM Analog Output (4/5)

- A low-pass filtered is required to eliminate the inherent noise components in PWM signal.
  - ❑ PWM signals contain strong noise components at the PWM frequency and at odd harmonics of that frequency.
- The output voltage is directly proportional to the pulse width.
  - ❑ By changing the pulse width of the PWM waveform, we can control the output voltage.

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PWM Analog Output (5/5)

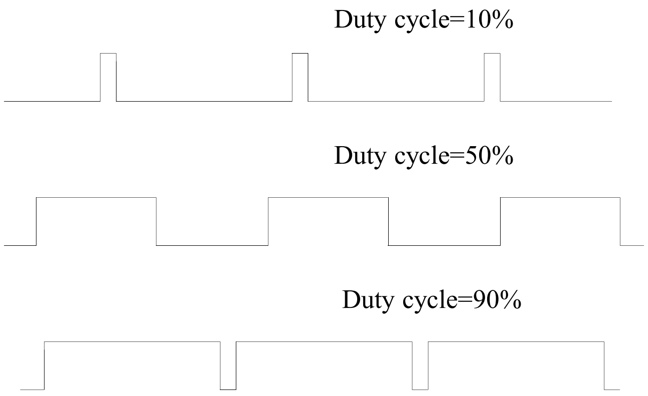
Pulse-width modulation uses a rectangular pulse wave. Consider a pulse waveform f(t) with a period T, a low value y_{min} (y_{min}=0), a high value y_{max}, and a duty cycle D, the average value y of the waveform is given by:

$$y=\frac{1}{T}\int_0^T f(t)\,dt$$

Since f(t) is a pulse wave, its value is y_{max} for $0<t<DT$ and y_{min} for $DT<t<T$, the above equation becomes:

$$\begin{aligned} y &= \frac{1}{T}\left(\int_0^{DT} y_{max}\,dt + \int_{DT}^{T} y_{min}\,dt\right) \\ &= \frac{1}{T}\left(DT y_{max} + T\,(1-D) y_{min}\right) \\ &= D y_{max} \end{aligned}$$

Examples of PWM Signals



PWM Generation in AVR

- Implemented via a timer/counter.
  - ❑ All the timers of ATmega2560 provide PWM wave generators.
- Two operation modes
  - ❑ Fast PWM mode
    - ❖ Details are covered later.
  - ❑ Phase correct PWM mode
    - ❖ Refer to ATmega2560 Data Sheet for details.

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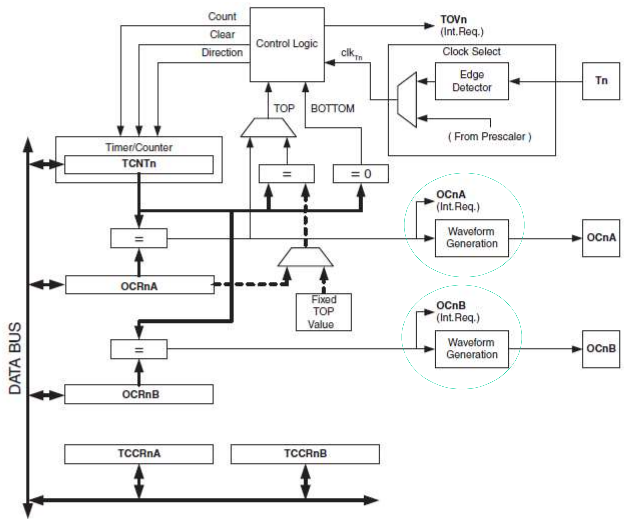
PWM Generation in Timer0 (1/3)



Two PWM wave form generators of Time/Counter 0

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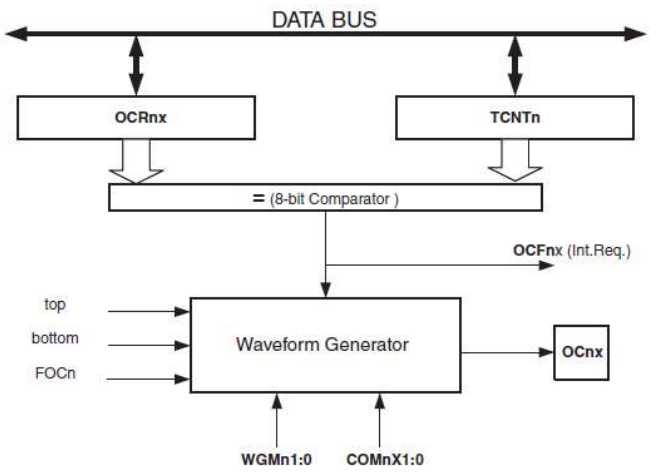
PWM Generation in Timer0 (2/3)



Block Diagram of Output Compare Unit (x=A, B)

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PWM Generation in Timer0 (3/3)

- The 8-bit comparator continuously compares TCNT0 (TCNT1) with the Output Compare Register OCR0A (OCR0B).
  - ❑ Whenever TCNT0 (TCNT1) equals OCR0A (OCR0B), the comparator signals a match.
  - ❑ The Waveform Generator uses the match signal to generate an output according to operating mode set by the WGM02:0 bits and Compare Output mode (COM0x1:0) bits.
- OC0A and OC0B pins generate PWM signals.

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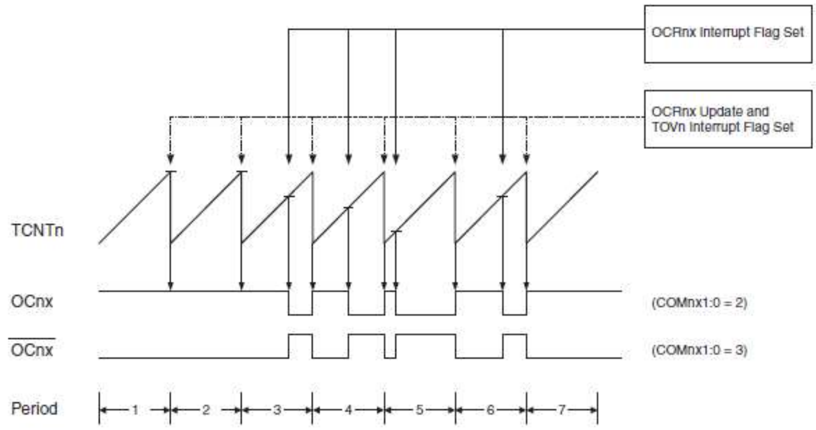
Fast PWM Mode (1/7)



Timing Diagram of Fast PWM Mode

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Fast PWM Mode (2/7)

• The fast PWM (WGM02:0=3 or 7) differs from the phase correct PWM mode by its single-slope operation.

• The counter counts from BOTTOM (0) to MAX (0xFF), then restarts from BOTTOM.

• In non-inverting Compare Output mode (COM0x1:0=2), the Output Compare (OC0x) is cleared on the Compare Match between TCNT0 and OCR0x, and set at BOTTOM.

• In inverting Compare Output mode (COM0x1:0=3) , the output is set on Compare Match and cleared at BOTTOM.

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Fast PWM Mode (3/7)

- Due to the single-slope operation, the operating frequency of the fast PWM mode can be twice as high as the phase correct PWM mode that uses dual-slope operation.
  - ❑ This high frequency makes the fast PWM mode well suited for power regulation, rectification, and DAC applications.

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Fast PWM Mode (4/7)

- Two Timer0 control registers TCCR0A and TCCR0B are used to control the settings of PWM wave generators of Timer0.

Bit	7	6	5	4	3	2	1	0	
0x24 (0x44)	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	TCCR0A
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0	
0x25 (0x45)	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	TCCR0B
Read/Write	W	W	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

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Fast PWM Mode (5/7)

Table 16-8. Waveform Generation Mode Bit Description

Mode	WGM2	WGM1	WGM0	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on[(1)(2)]
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	TOP	MAX
4	1	0	0	Reserved	–	–	–
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	–	–	–
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

Note: 1. MAX = 0xFF
2. BOTTOM = 0x00

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Fast PWM Mode (6/7)

Table 16-3. Compare Output Mode, Fast PWM Mode[(1)]

COM0A1	COM0A0	Description
0	0	Normal port operation, OC0A disconnected
0	1	WGM02 = 0: Normal Port Operation, OC0A Disconnected WGM02 = 1: Toggle OC0A on Compare Match
1	0	Clear OC0A on Compare Match, set OC0A at BOTTOM (non-inverting mode)
1	1	Set OC0A on Compare Match, clear OC0A at BOTTOM (inverting mode)

Table 16-6. Compare Output Mode, Fast PWM Mode[(1)]

COM0B1	COM0B0	Description
0	0	Normal port operation, OC0B disconnected
0	1	Reserved
1	0	Clear OC0B on Compare Match, set OC0B at BOTTOM (non-inverting mode)
1	1	Set OC0B on Compare Match, clear OC0B at BOTTOM (inverting mode)

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Fast PWM Mode (7/7)

• The duty cycle of a PWM signal generated by OC0A (OC0B) is determined by OCR0A, COM0A1 and COM0A0 (OCR0B, COM0B1 and COM0B0).

- ❑ Assume OCR0A is set to 0x1F and COM0A1:COM0A0=1:0 (non-inverting mode). The duty cycle of the PWM signal generated by the pin OC0A is (0x1F/256)*100% ≈12.1%

Reading

1. Chapter 11: Analog Input and Output. Microcontrollers and Microcomputers by Fredrick M. Cady.
2. Timer/Counter0. AVR Mega2560 Data Sheet.