Analog Input and Output

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Lecture overview

- Analog output
  - PWM
  - Digital-to-Analog (D/A) Conversion
- Analog input
  - Analog-to-Digital (A/D) Conversion

PWM Analog Output

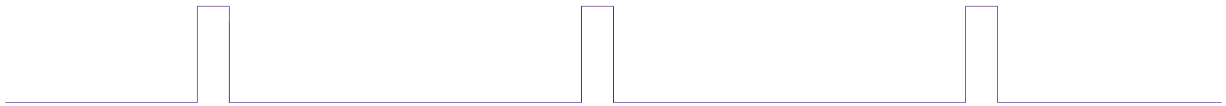
- PWM (Pulse Width Modulation) is a way of digitally encoding analog signal levels.
  - Through the use of high-resolution counters, the duty cycle (pulse width/period) of a pulse wave is modulated to encode a specific analog signal level.
- The PWM signal is still digital
  - Its value is either full high or full low.
  - Given a sufficient bandwidth, any analog value can be encoded with PWM.
- PWM is a powerful technique for controlling analog circuits with a processor's digital outputs.
- It is employed in a wide variety of applications
  - E.g. motor speed control

PWM Analog Output (cont.)

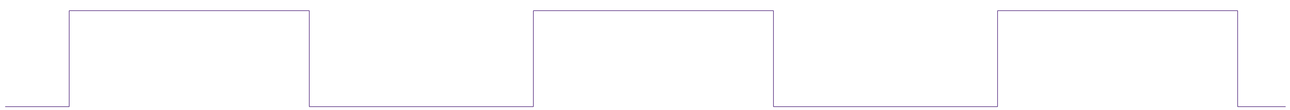
- A low-pass filtered is required to smooth the input signal and eliminate the inherent noise components in PWM signal.
- The output voltage is directly proportional to the pulse width.
  - By changing the pulse width of the PWM waveform, we can control the output value.

Examples of PWM Signals

Duty cycle=10%



Duty cycle=50%

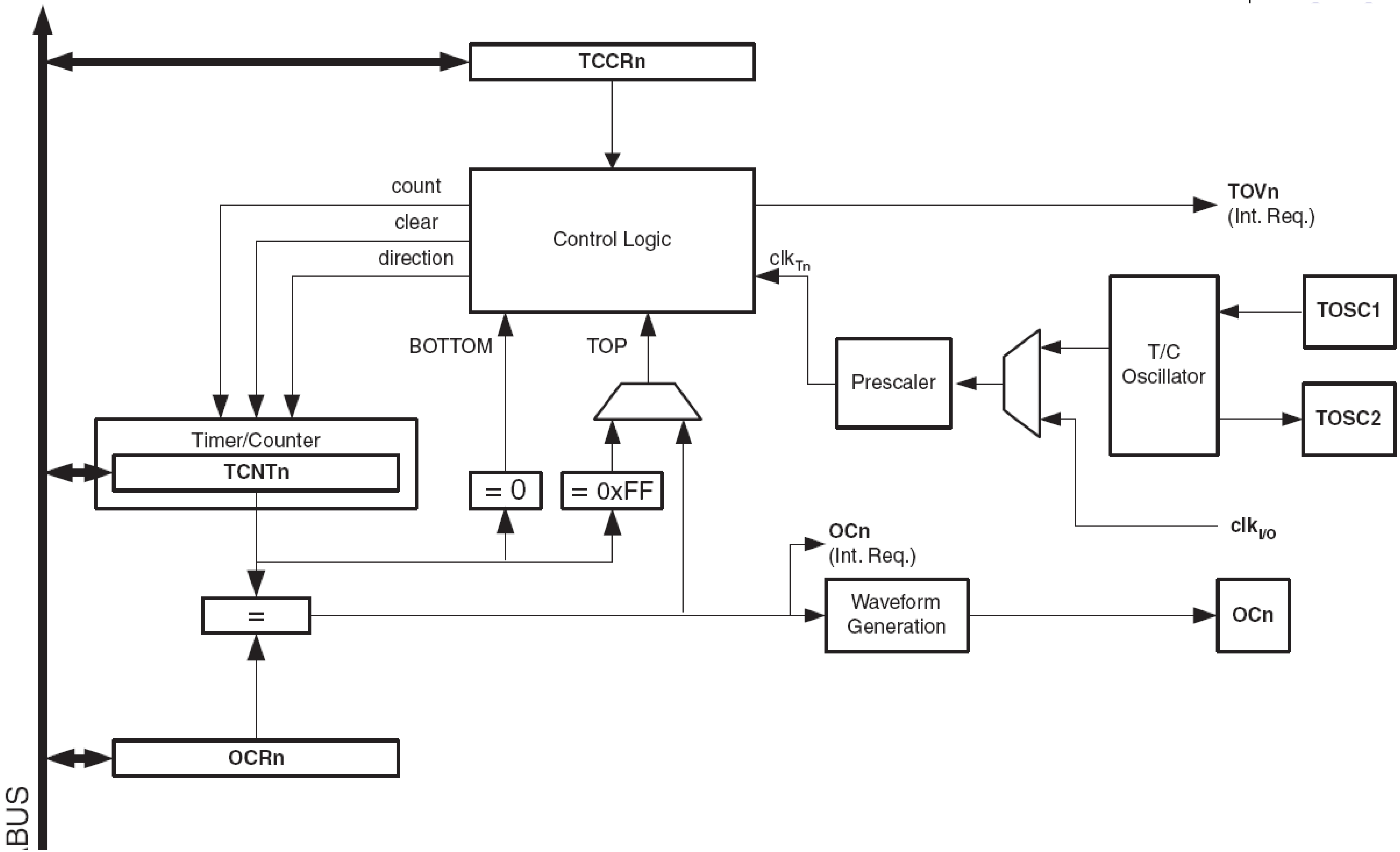


Duty cycle=90%

PWM Generation In AVR

- PWM can be obtained through the provided timers.

Recall: Timer0



Configuration for PWM

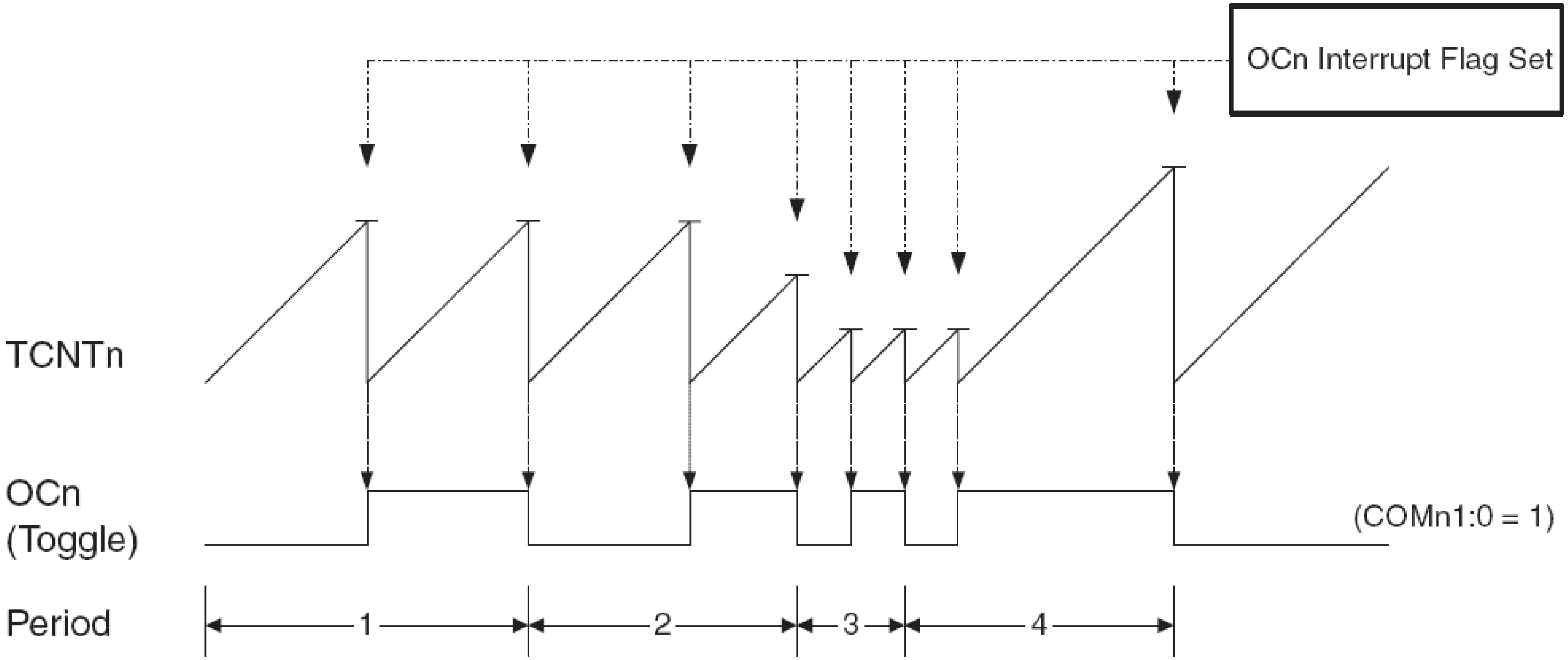
- TCCR0A

Bit	7	6	5	4	3	2	1	0	
0x24 (0x44)	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	TCCR0A
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

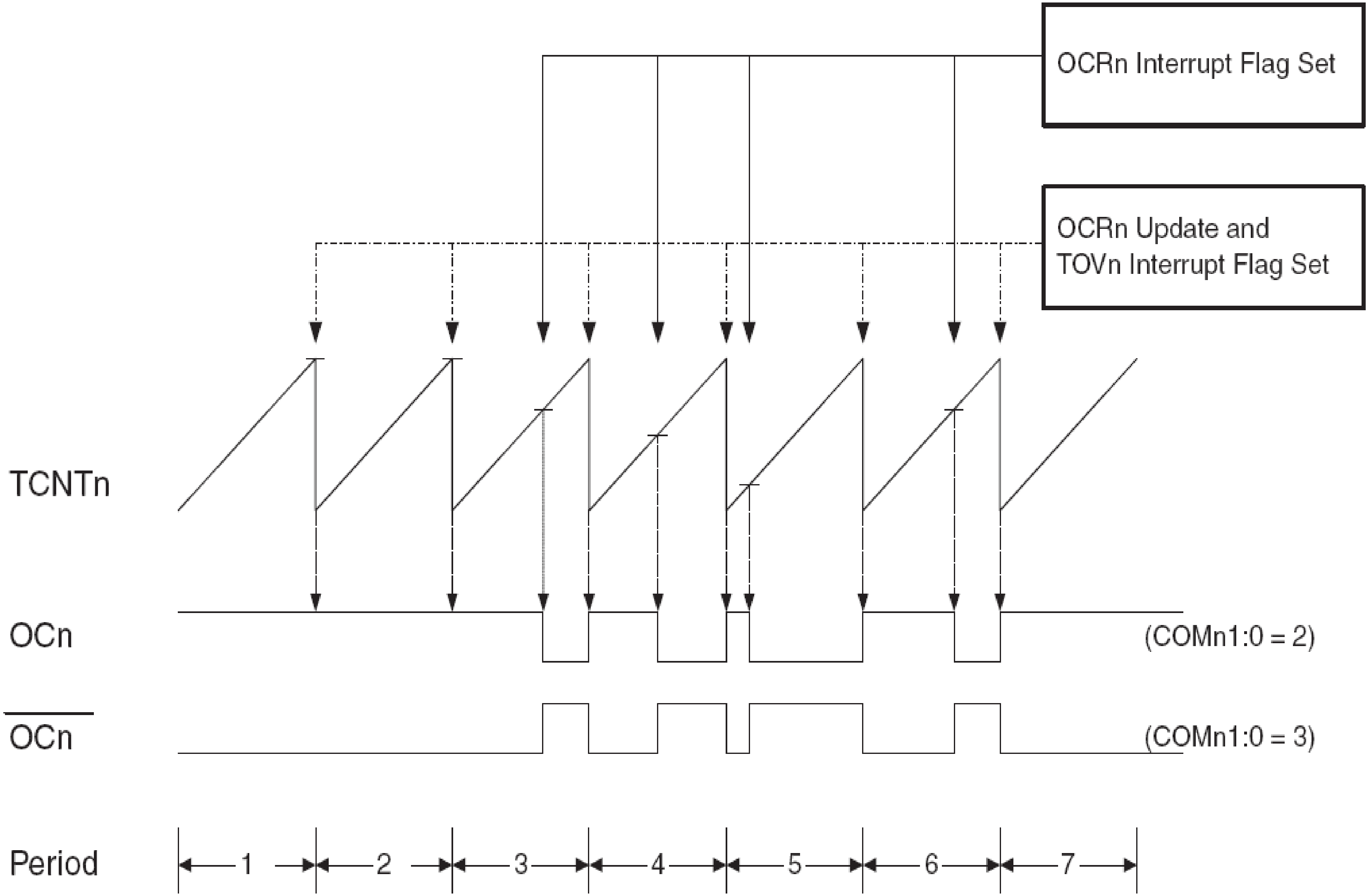
Mode	WGM2	WGM1	WGM0	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on[(1)(2)]
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	TOP	MAX
4	1	0	0	Reserved	–	–	–
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	–	–	–
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

CTC

- Clear Timer on Compare Match

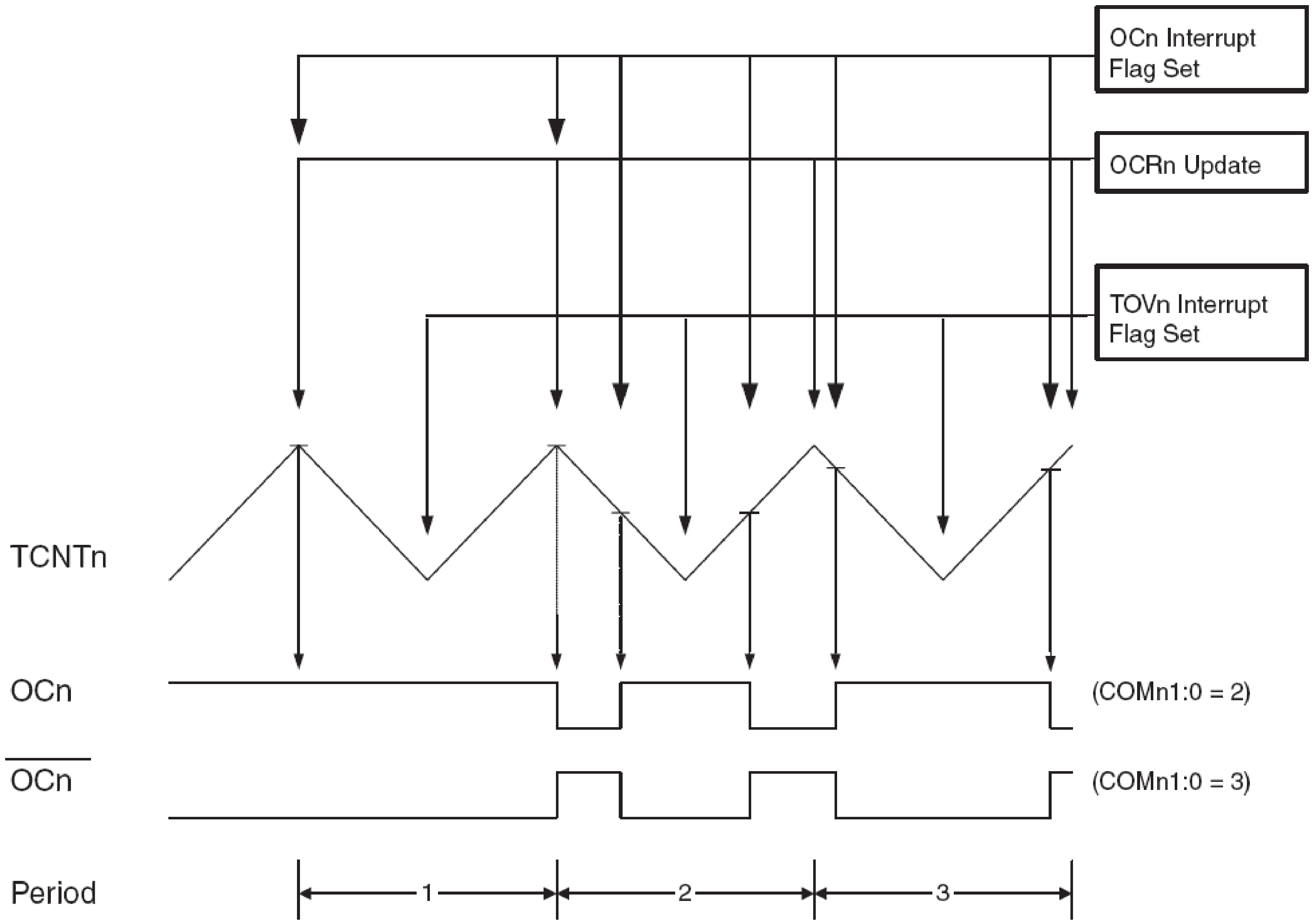


Fast PWM



OCRn Interrupt Flag Set
OCRn Update and
TOVn Interrupt Flag Set
TCNTn
OCn
(COMn1:0 = 2)
OCn
(COMn1:0 = 3)
Period
1
2
3
4
5
6
7

Phase Correct PWM



Example

- Generate a PWM waveform.

Example (solution)

- Use Timer5
  - Set OC5A as output
  - Set the Timer5 operation mode as Phase Correct PWM mode
  - Set the timer clock

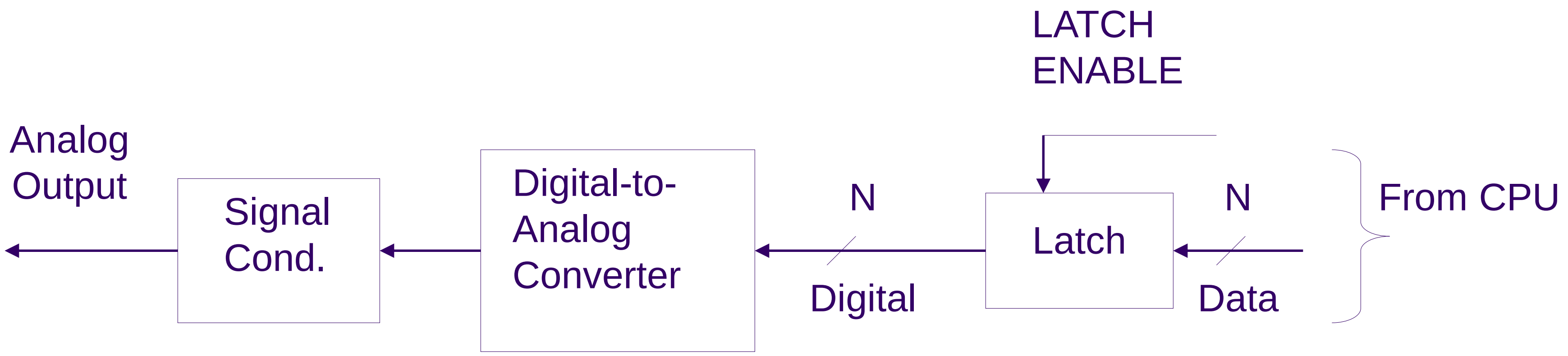
Example Code

```
.include "m2560def.inc"
.def temp = r16

       ldi temp, 0b00001000
       sts DDRL, temp          ; Bit 3 will function as OC5A.

       ldi temp, 0x4A          ; the value controls the PWM duty cycle
       sts OCR5AL, temp
       clr temp
       sts OCR5AH, temp
                        ; Set the Timer5 to Phase Correct PWM mode.
       ldi temp, (1 << CS50)
       sts TCCR5B, temp
       ldi temp, (1<< WGM50)|(1<<COM5A1)
       sts TCCR5A, temp
halt:
       rjmp halt
```

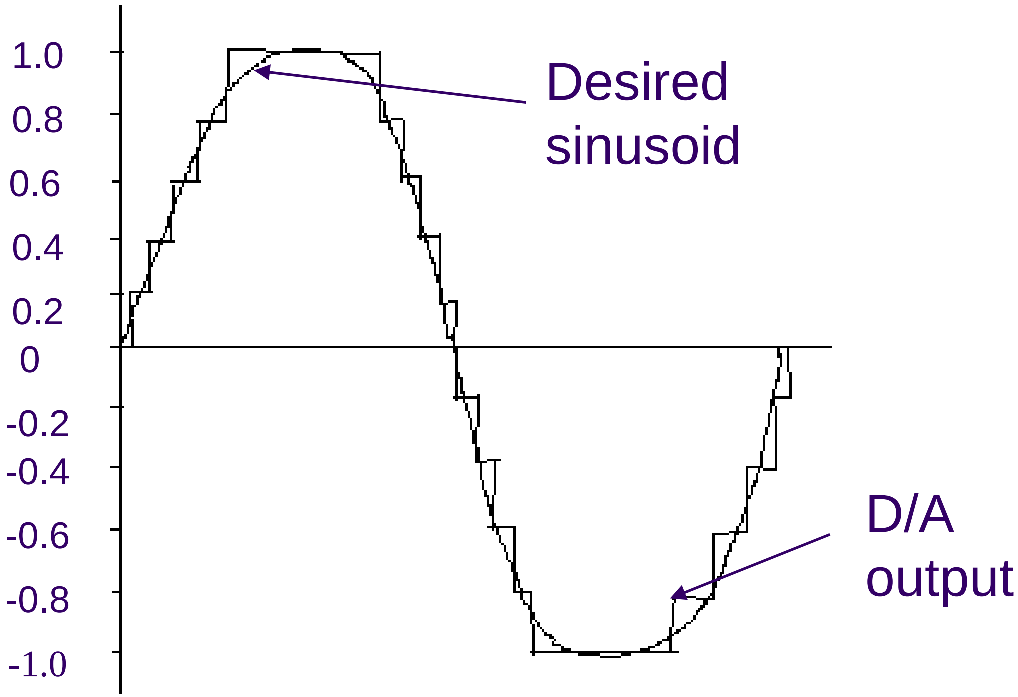
Digital-to-Analog Conversion



Digital-to-Analog Conversion (cont.)

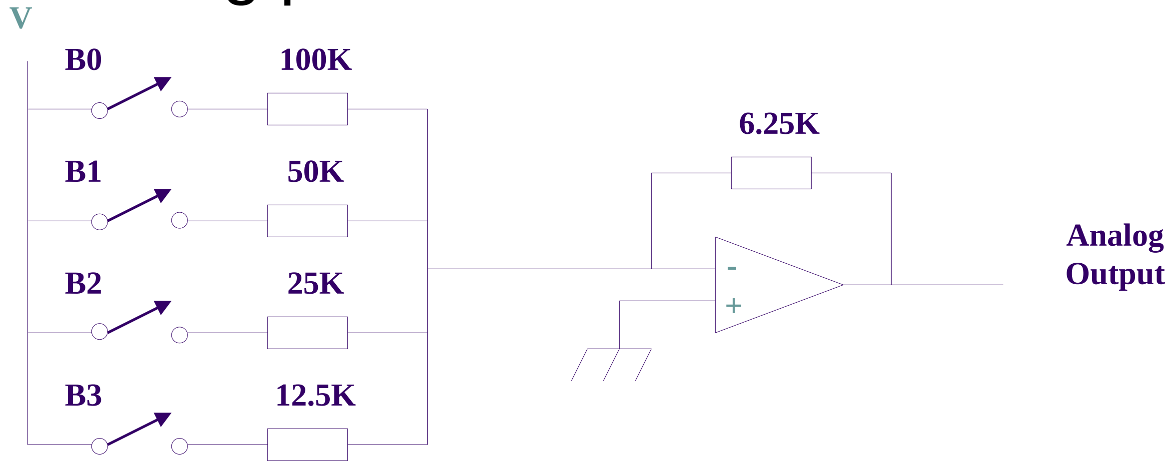
- A parallel output interface connects the D/A to the CPU.
- The latches may be part of the D/A converter or the output interface.
- Digital value is converted into continuous value.
- A signal conditioning block may be used as a filter to smooth the quantized nature of the output.
  - The signal conditioning block also provide isolation, buffering and voltage amplification if needed.

Quantized D/A Output



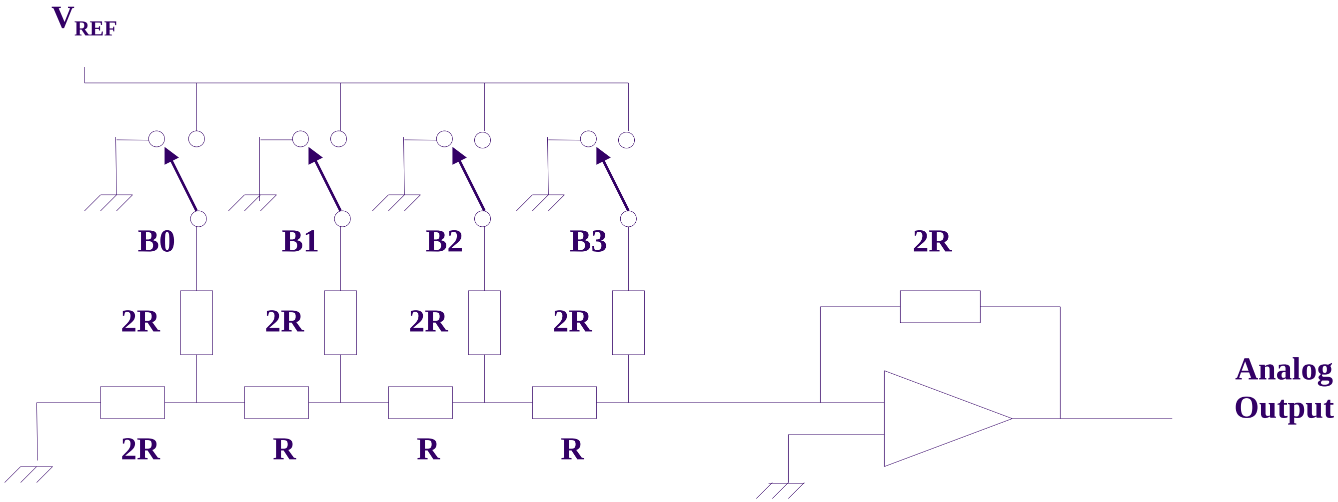
Binary-weighted D/A Converter

- As the switches for the bits are closed, a weighted current is supplied to the summing junction of the amplifier.
- For high-resolution D/A converters, the binary-weighted type must have a wide range of resistors. This may lead to temperature stability and switching problems.



R-2R Ladder D/A Converter

- As the switches for the grounded to the reference position, a binary-weighted current is supplied to the summing junction.
- For high-resolution D/A converters, a wide range of resistors are not required.



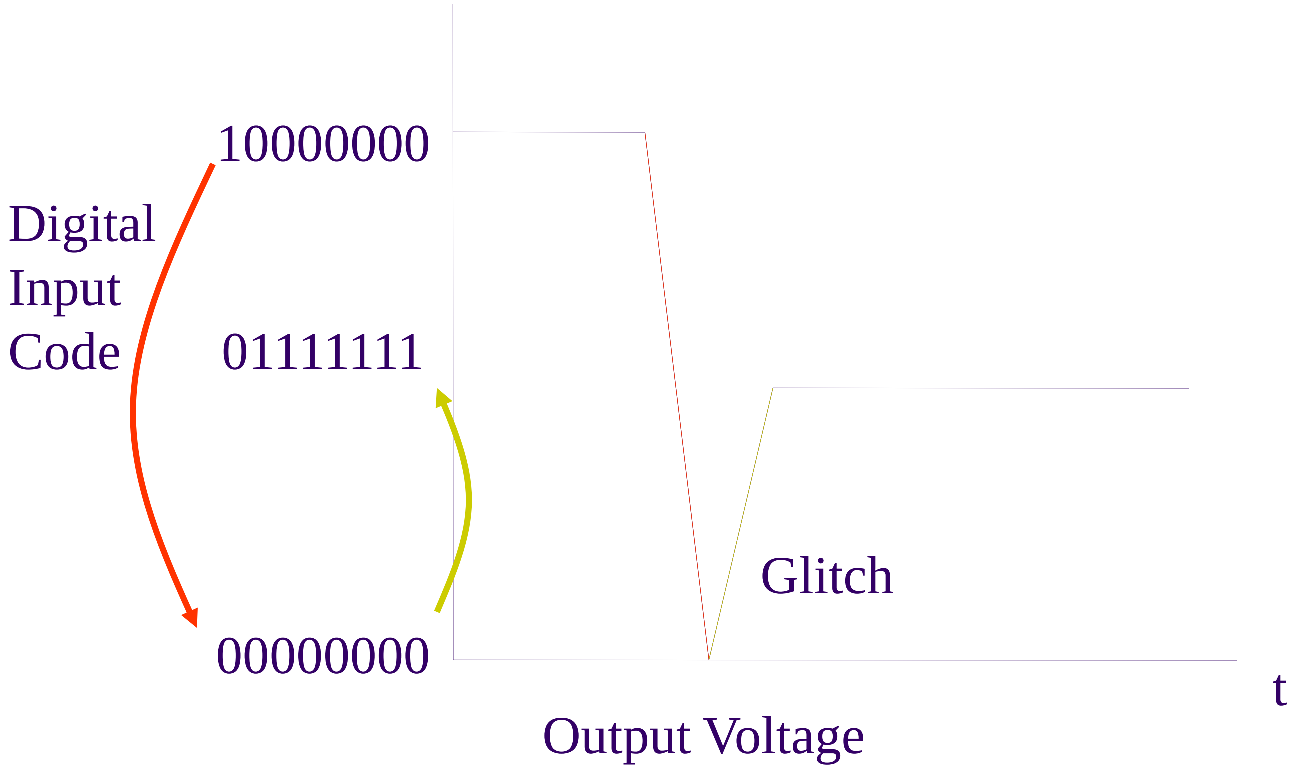
D/A Converter Specifications

- Resolution and linearity.
  - The resolution is determined by the number of bits and is given as the output voltage corresponding to the smallest digital step, i.e. 1 LSB.
  - The linearity shows how closely the output voltage to the idea values (a straight line drawn through zero and full-scale).
- Settling Time.
  - The time taken for the output voltage to settle to within a specified error band, usually ± ½ LSB.

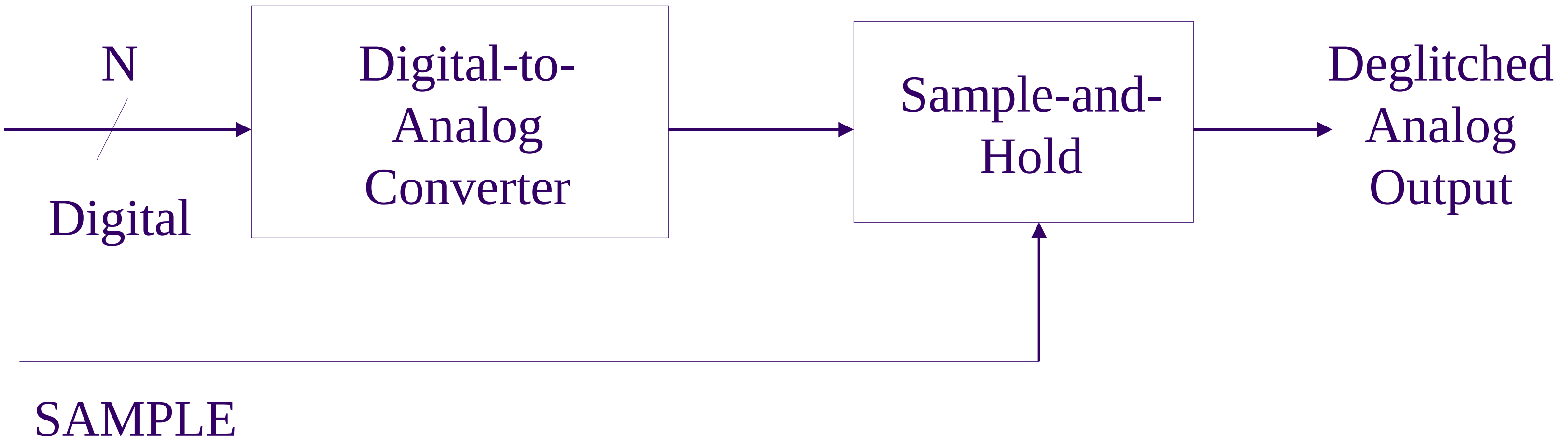
D/A Converter Specifications (cont.)

- Glitches.
  - A glitch is caused by asymmetrical switching in the D/A switches. If a switch changes from a one to a zero faster than from a zero to a one, a glitch may occur.
    - Consider changing the output code of a 8-bit D/A from 10000000 to 01111111 in the next slide.
  - D/A converter glitch can be eliminated by using a sample-and-hold.

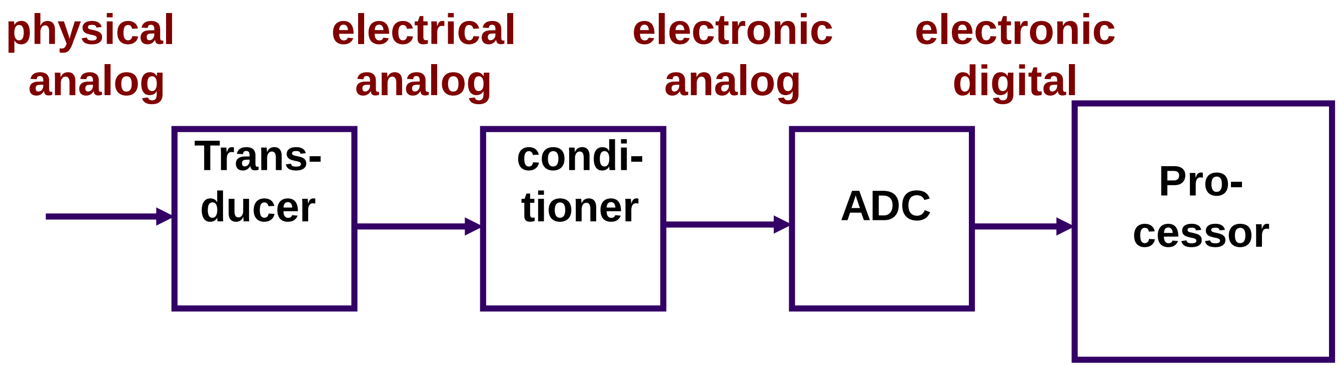
D/A Output Glitch



Deglitched D/A



A/D Conversion



Data Acquisition and Conversion

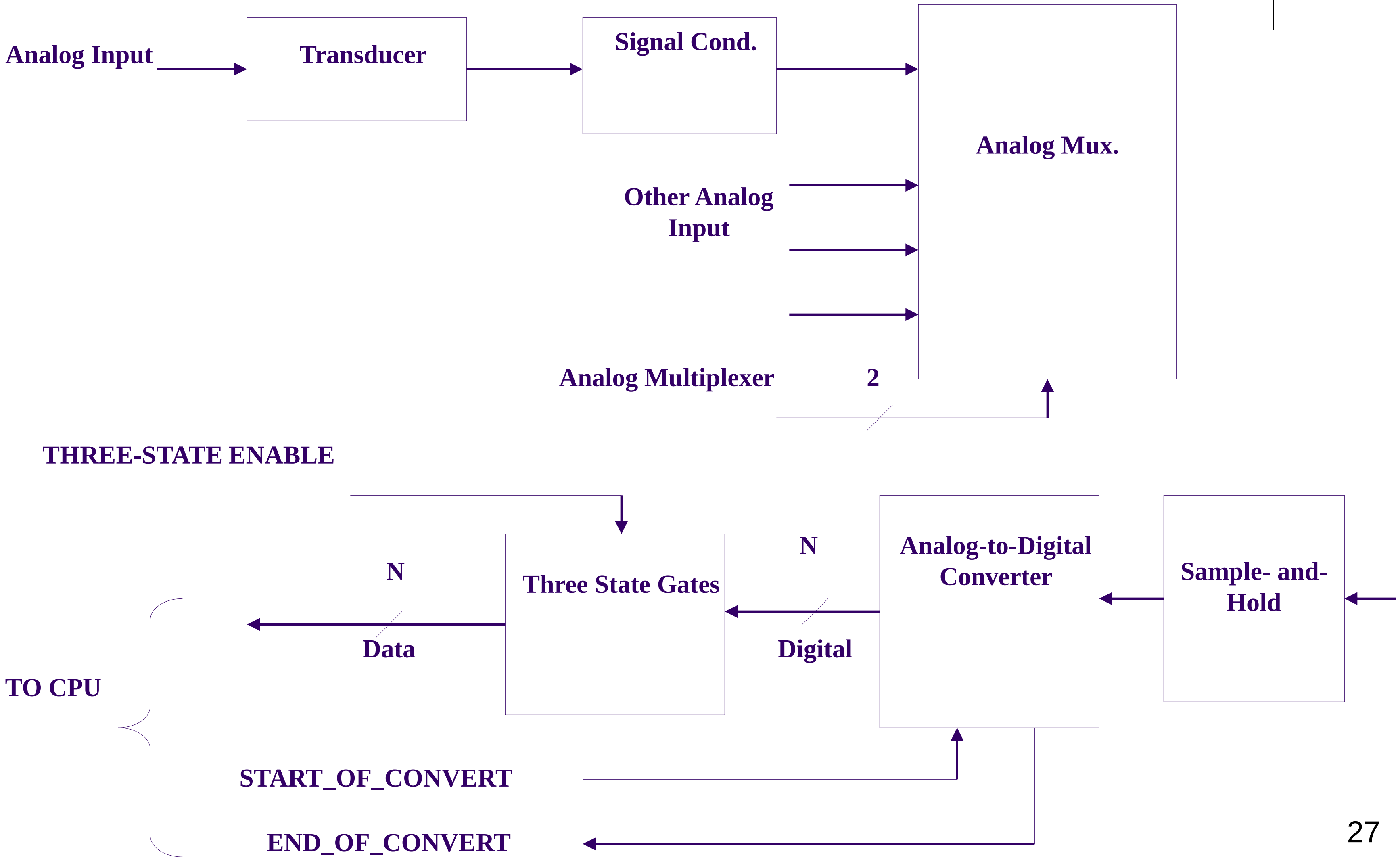
Procedure of data acquisition and conversion:

- A transducer converts physical values to electrical signals, either voltages or currents.
- Signal conditioner performs the following tasks:
  - Isolation and buffering: The input to the A/D may need to be protected from dangerous voltages such as static charges or reversed polarity voltages.
  - Amplification: Rarely does the transducer produce the voltage or current needed by the A/D. The amplifier is designed so that the full-scale signal from the analog results in a full-scale signal to the A/D.
  - Bandwidth limiting: The signal conditioning provides a low-pass filter to limit the range of frequencies that can be digitized.

Data Acquisition and Conversion (Cont.)

- In applications where several analog inputs must be digitized, an analog multiplexer is followed the signal conditioning. It allows multiple analog inputs, each with its own signal conditioning for different transducers.
- The sample-and-hold circuit samples the signal and holds it steady while the A/D converts it.
- The A/D converter converts the sampled signal to digital values.
- The three state gates hold the digital values generated by the A/D converter.

Data Acquisition System



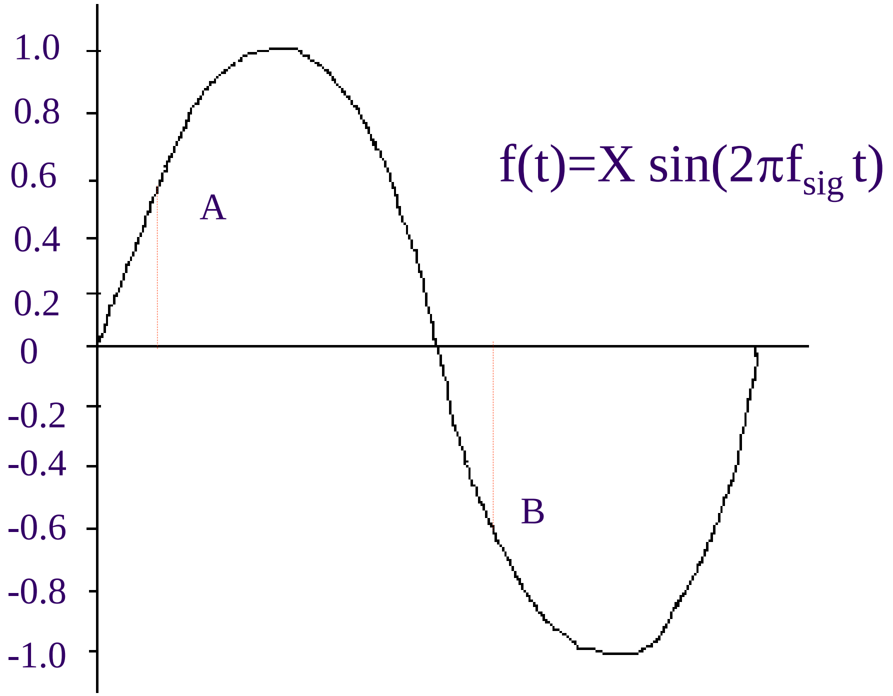
Shannon's Sampling Theorem

Claude Shannon's Theorem:

- When a signal, $f(t) = X \sin(2\pi f_{sig} t)$, is to be sampled (digitized), the minimum sampling frequency must be twice the signal frequency.

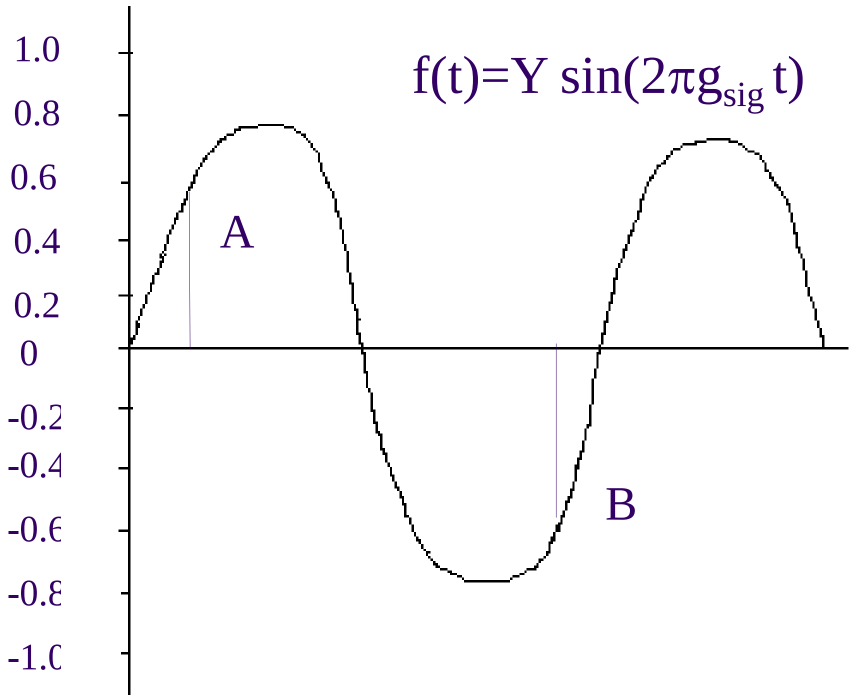
Sample Examples

- Sampled at twice of the signal frequency.



Sample Examples

- Under-sampled, with sample frequency less than twice of the signal frequency

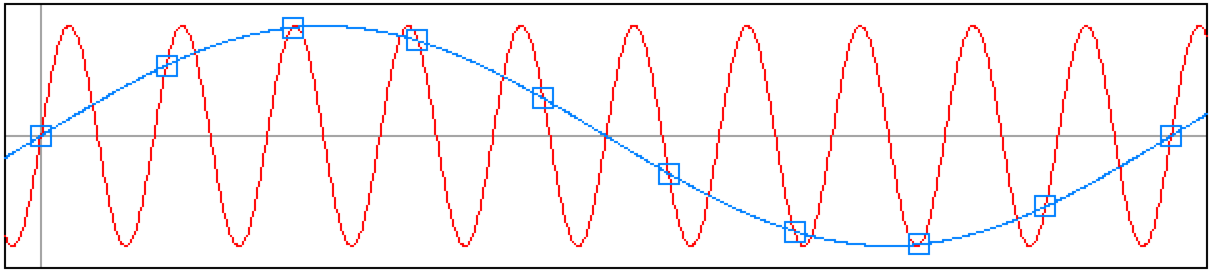


Shannon's Sampling Theorem and Aliasing

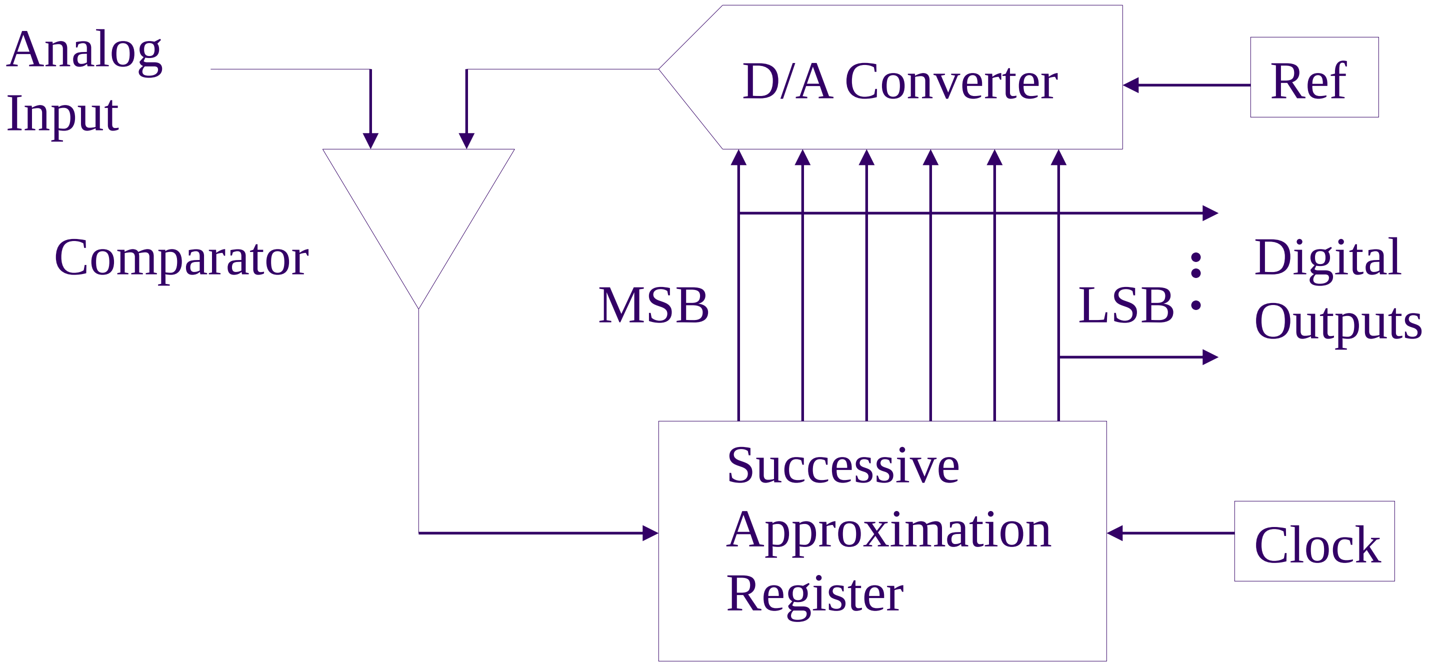
- To preserve the full information in the signal, it is necessary to sample at twice the maximum frequency of the signal. This is known as the *Nyquist rate*.
- A signal can be exactly reproduced if it is sampled at a frequency F, where F is greater than or equal to the Nyquist rate.
- If the sampling frequency is less than Nyquist rate, the waveform is said to be under-sampled.

Shannon's Sampling Theorem and Aliasing (Cont.)

- Undersampled signal, when converted back into a continuous time signal, will exhibit a phenomenon called *aliasing*.
  - Aliasing is the presence of unwanted components in the reconstructed signal. These components were not present when the original signal was sampled.



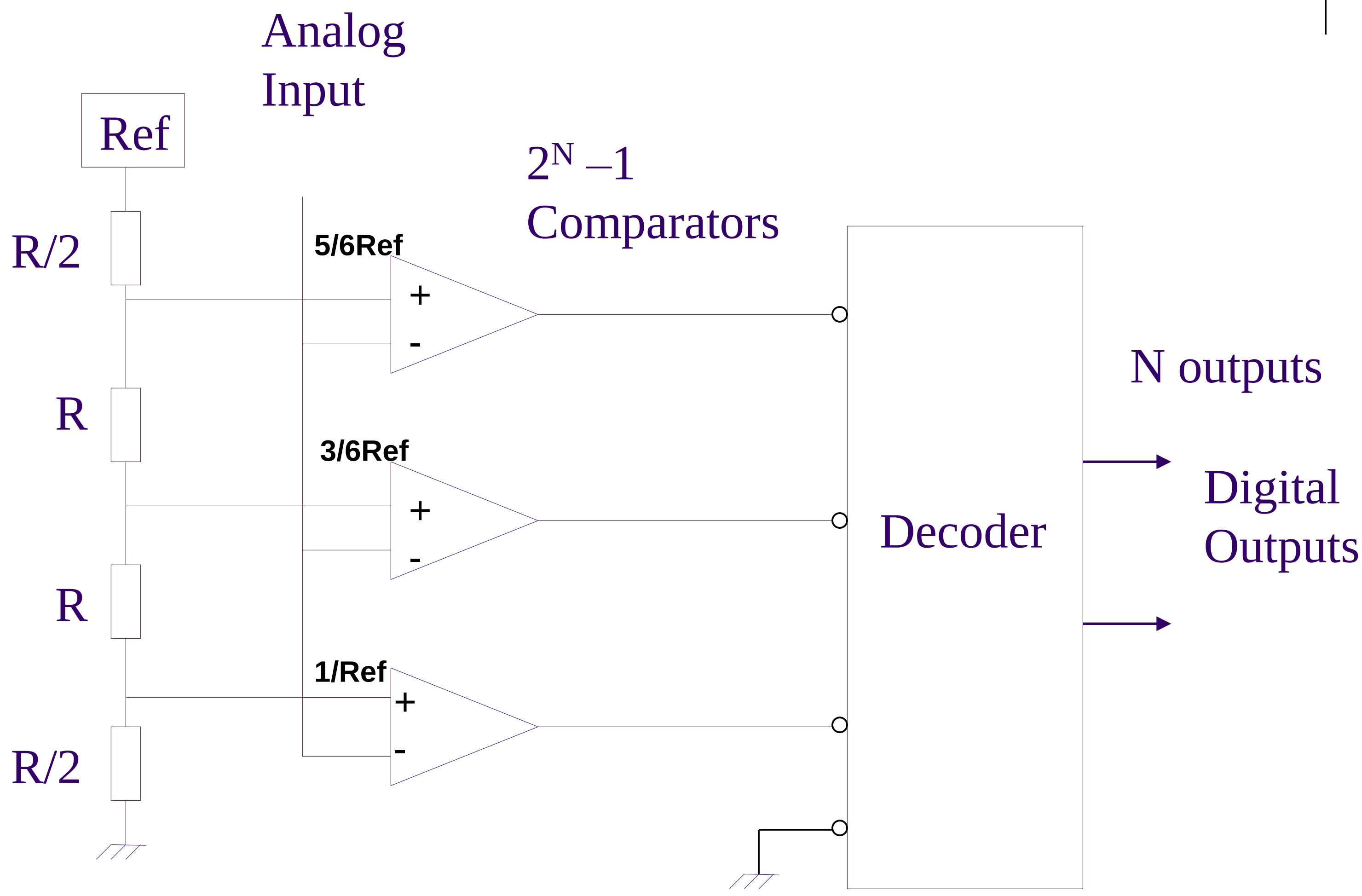
Successive Approximation Converter



Successive Approximation A/D Converter

- Each bit in the successive approximation register is tested, starting at the most significant bit and working toward the least significant bit.
- As each bit is set, the output of the D/A converter is compared with the input.
- If the D/A output is lower than the input signal, the bit remains set and the next bit is tried.
- N times are required to set and test each bit in the successive approximation register.

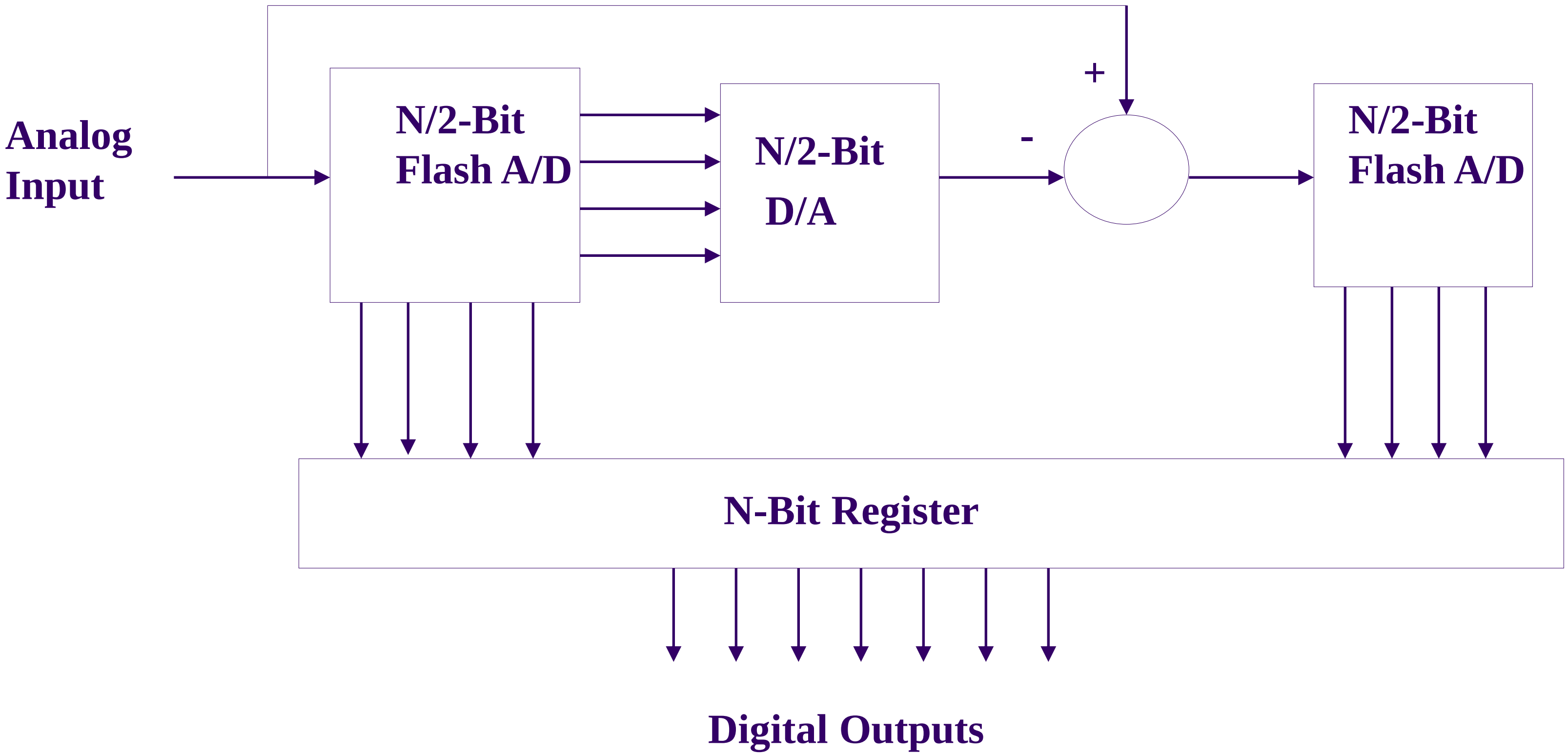
Parallel A/D Converter



Parallel A/D Converter

- An array of 2^N-1 comparators and produces an output code in the propagation time of the comparators and the output decoder.
- Fast but more costly in comparison to other designs.
- Also called flash A/D converter.

Two-Stage Parallel A/D Converter



Two-Stage Parallel A/D Converter

- The input signal is converted in two pieces.
  - First, a coarse estimate is found by the first parallel A/D converter. This digital value is sent to the D/A and summer, where it is subtracted from original signal.
  - The difference is converted by the second parallel converter and the result combined with the first A/D to give the digitized value.
- It has nearly the performance of the parallel converter but without the complexity of $2^N - 1$ comparators.
- It offers high resolution and high-speed conversion for applications like video signal processing.

A/D Converter Specifications

- Conversion time
  - The time required to complete a conversion of the input signal.
  - Establishes the upper signal frequency limit that can be sampled without aliasing.

$$f_{MAX}=1/(2*\text{conversion time}) \qquad (1)$$

- Resolution
  - The number of bits in the converter gives the resolution and thus the smallest analog input signal for which the converter will produce a digital code.
  - It may be given in terms of the full-scale input signal:

$$\text{Resolution}=\text{full-scale signal}/2^n \qquad (2)$$

  - It is often given as the number of bits, n; or stated as one part in 2^n.
  - Sometimes it is given as a percent of maximum.

A/D Converter Specifications (Cont.)

- Accuracy
  - Relates to the smallest signal (or noise) to the measured signal.
  - Given as a percent and describes how close the measurement is to the actual value.

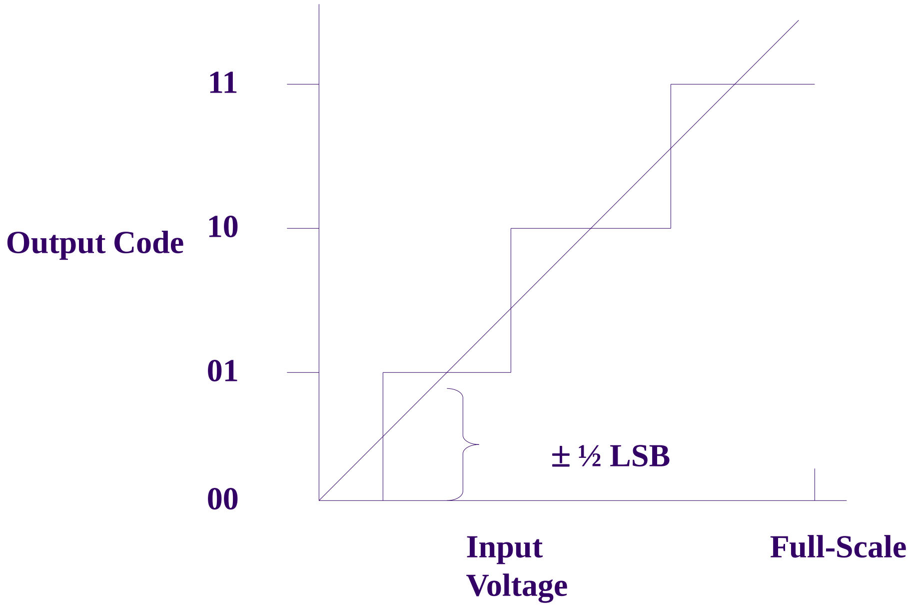
  The signal is accurate to within 100% * $V_{RESOLUTION}/V_{SIGNAL}$ (3)
- Linearity
  - The derivation in output codes from the real value (a straight line drawn through zero and full-scale).
  - The best that can be achieved is ± ½ of the least significant bit

    (± ½ LSB).

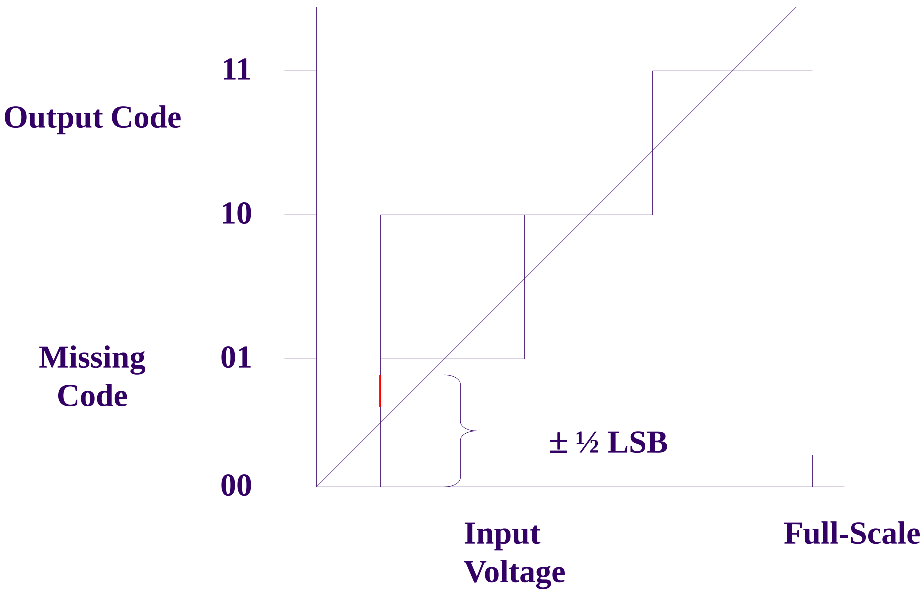
A/D Converter Specifications (Cont.)

- Missing codes.
  - A missing code could be caused by an internal error, especially by the D/A converter in a successive approximation converter.
- Aperture time.
  - The time that the A/D converter is “looking” at the input signal.
  - It is usually equal to the conversion time.

A/D Converter Specifications (Cont.)



A/D linearity



A/D missing codes

A/D Errors

- Three sources of errors in A/D conversion:
- Noise:
  - All signals have noise.
  - Need to reduce noise or choose the converter resolution appropriately to control the peak-to-peak noise.
- Aliasing:
  - The errors due to aliasing is difficult to quantify.
  - They depend on the relative amplitude of the signals at frequencies below and above the Nyquist frequency.
  - The system design should include a low-pass filter to attenuate frequencies above the Nyquist frequency.

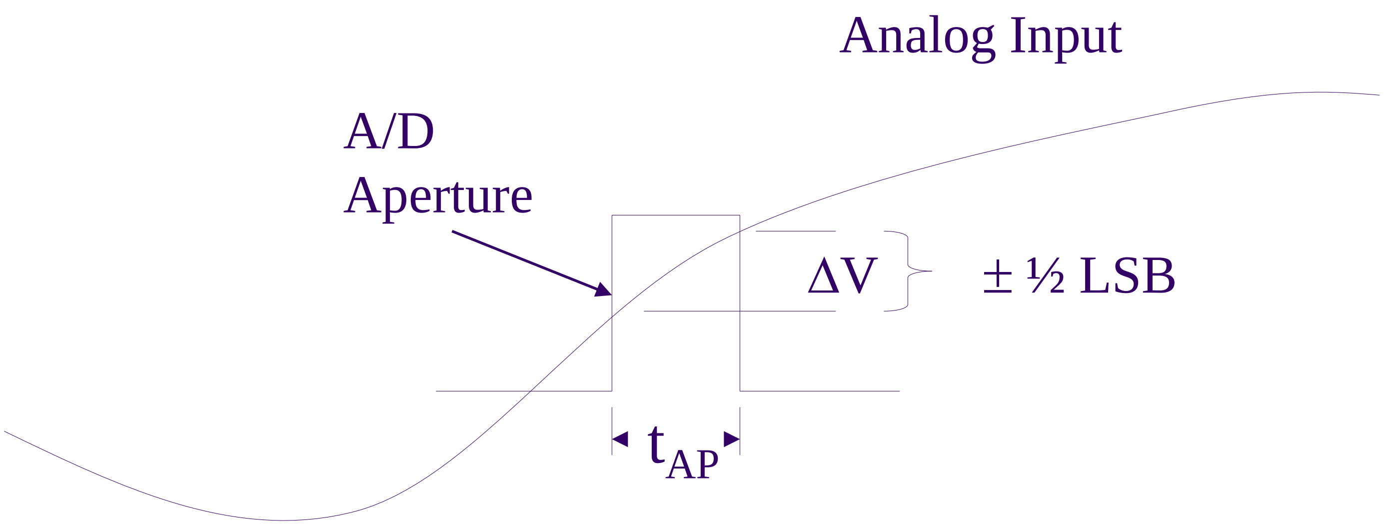
A/D Errors (cont.)

- Aperture.
  - A significant error in a digitizing system is due to signal variation during the aperture time.
  - A good design will attempt to have the uncertainty, ΔV, be less than one least significant bit.
  - A design equation for the aperture time, t_{AP}, in terms of the maximum signal frequency, f_{MAX}, and the number of bits in the A/D converter is

$$t_{AP} = 1/(2 \pi f_{MAX} 2^n) \qquad (4)$$

  - The aperture time needed to reduce the error to is surprisingly short.

A/D Errors (Cont.)



Aperture time error

Reading Material

- Chapter 11: Analog Input and Output. Microcontrollers and Microcomputers by Fredrick M. Cady.
- Timers/Counters. AVR Mega2560 Data Sheet.
  - PWM

Homework

1. With the AVR lab board, connect PB7 to a LED and run the following code. What did you observe?

```
.include "m2560def.inc"
.def temp=r16

ldi temp, 0b00001000
sts DDRL, temp ; Bit 3 will function as OC5A.

ldi temp, 0x4A          ; the value controls the PWM duty cycle
sts OCR5AL, temp
clr temp
sts OCR5AH, temp
                        ; Set the Timer5 to Phase Correct PWM mode.
ldi temp, (1 << CS50)
sts TCCR5B, temp
ldi temp, (1<< WGM50)|(1<<COM5A1)
sts TCCR5A, temp
```

Homework

2. The A/D converter conversion time is 100 us. What is the maximum frequency that can be digitalized without aliasing occurring?

Homework

3. A transducer is to be used to find the temperature over a range of –100 to 100^{o}C. We are required to read and display the temperature to a resolution of +/- 1^{o}C. The transducer produces a voltage from –5 to +5 volts over this temperature range with 5 millivolts of noise. Specify the number of bits in the A/D converter (a) based on the dynamic range and (b) based on the required resolution.