DESN2000 (Computer Engineering)

Analogue to Digital Converter

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So far

- GPIO
- I/O devices
- Interrupts
- Timers
- PWM

Upcoming

- ADC – today
- This Friday – help session for the project (Feddrick and Suneth)
- 8th week – PCB design and stepper motors (Hammond Pearce)
- 9th week – serial communication
- 10th week – advance content

Today

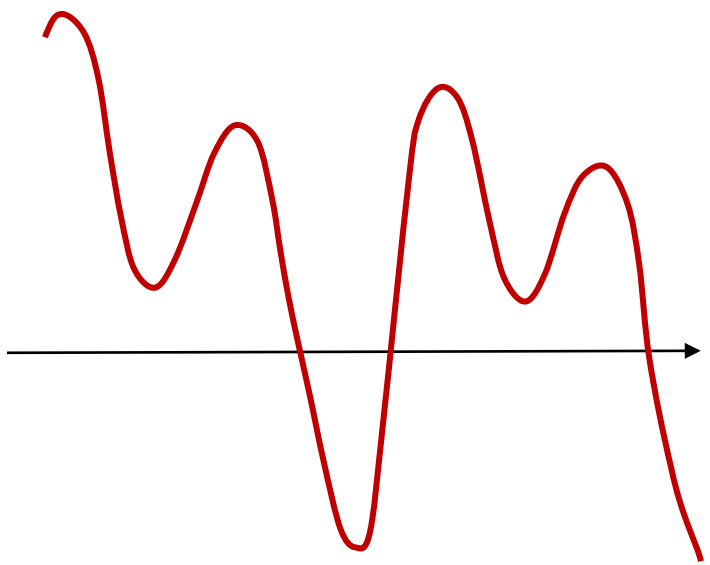
- A hands-on example of using a serial port (details covered in week 9)
- Basic ADC theory
- Basic ADC example
- Advanced ADC theory and examples (if time permits)

Learning Resources

The upcoming slides are adapted from “Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C (Fourth Edition)” – Yifeng Zhu

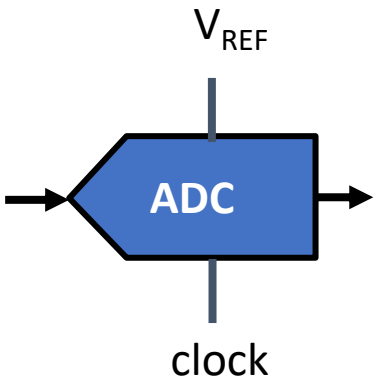
- Analog input and output - chapter 18

Analog-to-Digital Converter (ADC)

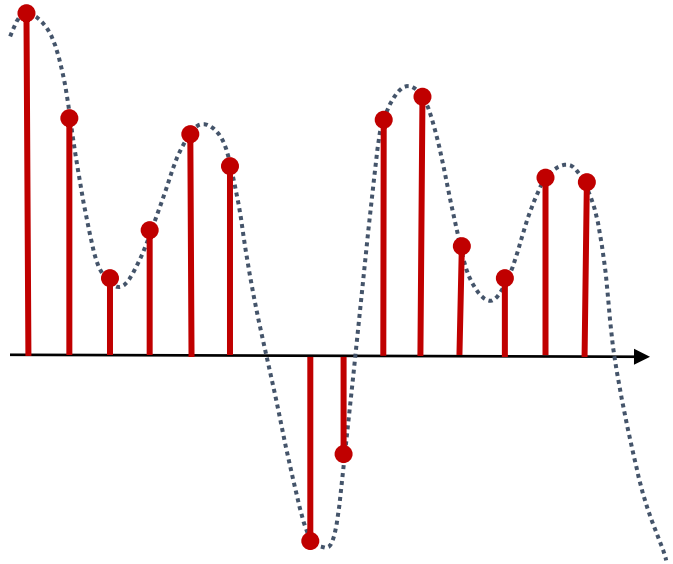


Analog signal $x(t)$

continuous time
continuous amplitude



- Resolution
- Quantization error
- Sampling rate

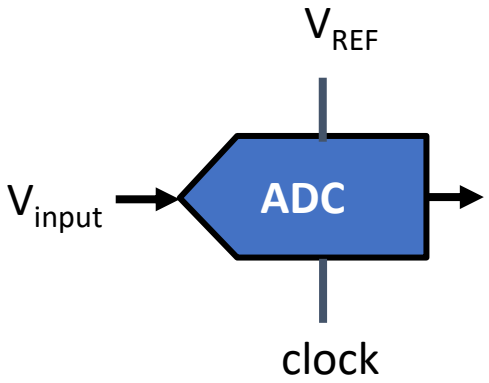


Digital values $x(n)$

discrete time
discrete amplitude

ADC: Resolution

- Resolution: number of binary bits in ADC output.



$$ADC\ Output = round\left((2^N - 1) \times \frac{V_{input}}{V_{REF}}\right)$$

- **N**: resolution
- **V_{REF}**: the maximum input voltage that can be converted by the ADC

Example: for 10-bit ADC, V_{input} = 1V, V_{REF} = 5V

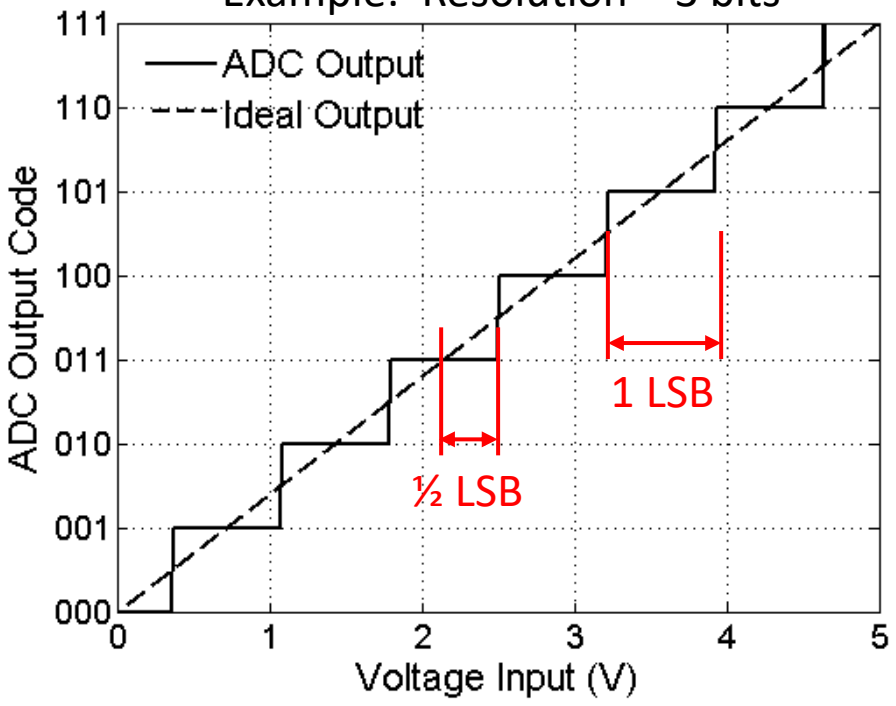
$$ADC\ Output = round\left(1023 \times \frac{1}{5}\right) = round(204.6) = 205 = 0xCD$$

ADC: Quantization Error

- Resolution N: number of binary bits in ADC output.

$$Digital\ Result = round\left((2^N - 1) \times \frac{V_{input}}{V_{REF}}\right)$$

Example: Resolution = 3 bits



Least significant bit (LSB) voltage

$$LSB = \frac{V_{REF}}{2^N - 1}$$

Max quantization error = ±½ LSB

Example: 3-bit ADC and input range [0, 5V]

$$Max\ Quantization\ Error = \pm\frac{1}{2}LSB$$

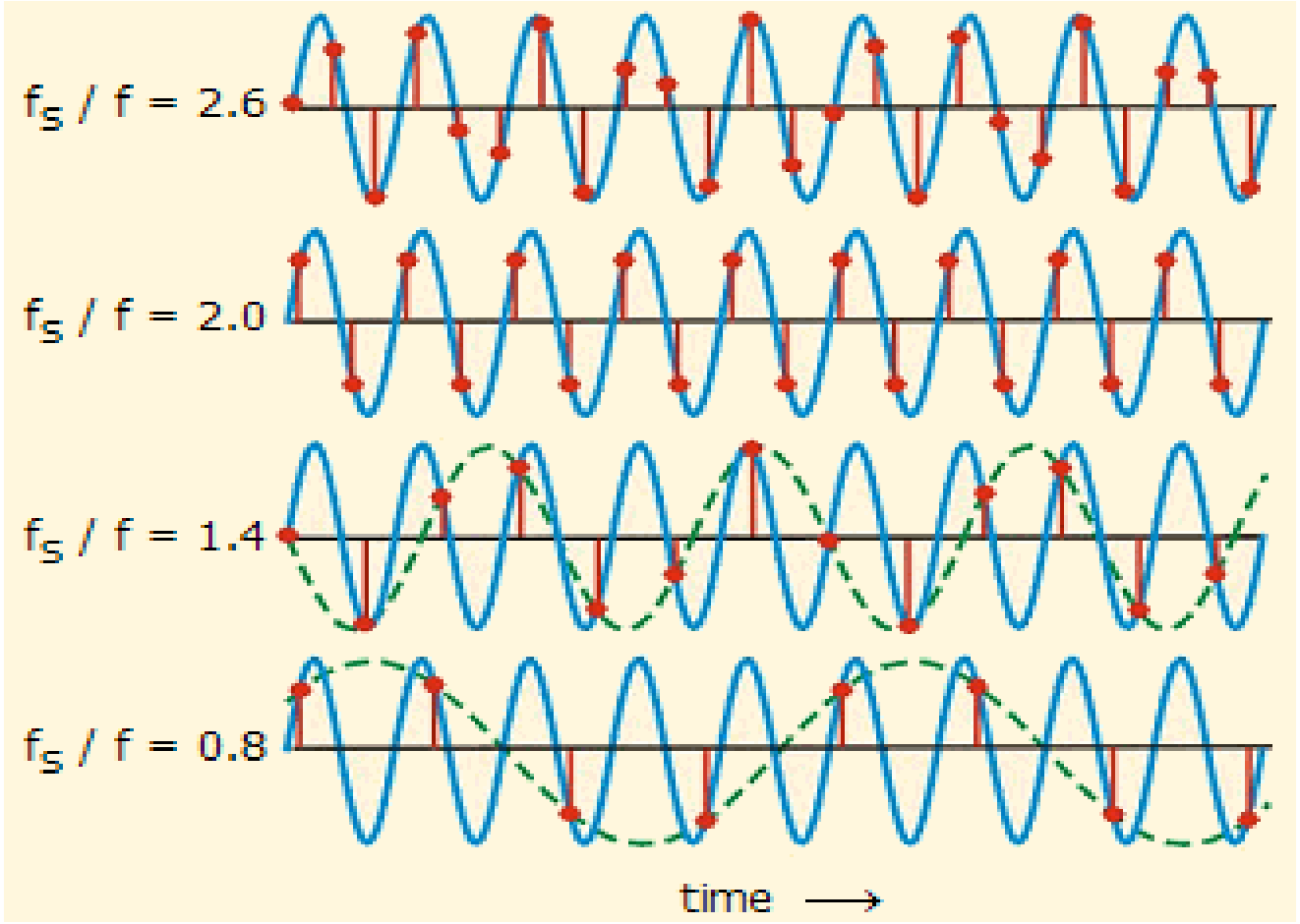
$$= \pm\frac{5V}{2 \times (2^3 - 1)}$$

$$= \pm 0.357\ V$$

What sampling rate do we need?

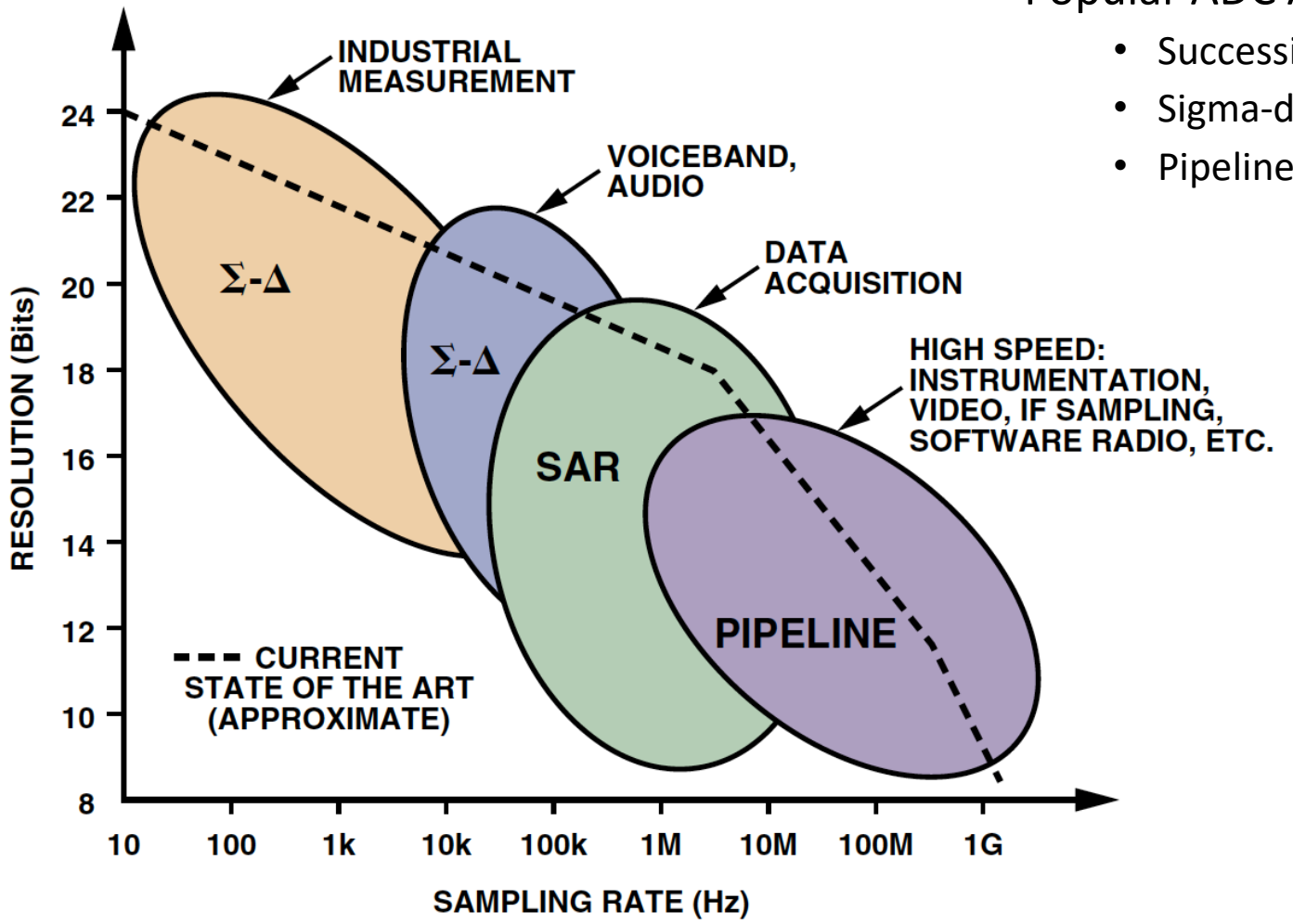
Nyquist–Shannon Sampling Theorem

$$f_{sampling} \geq 2 \cdot f_{signal}$$



http://195.134.76.37/applets/AppletNyquist/Appl_Nyquist2.html

ADC Architecture

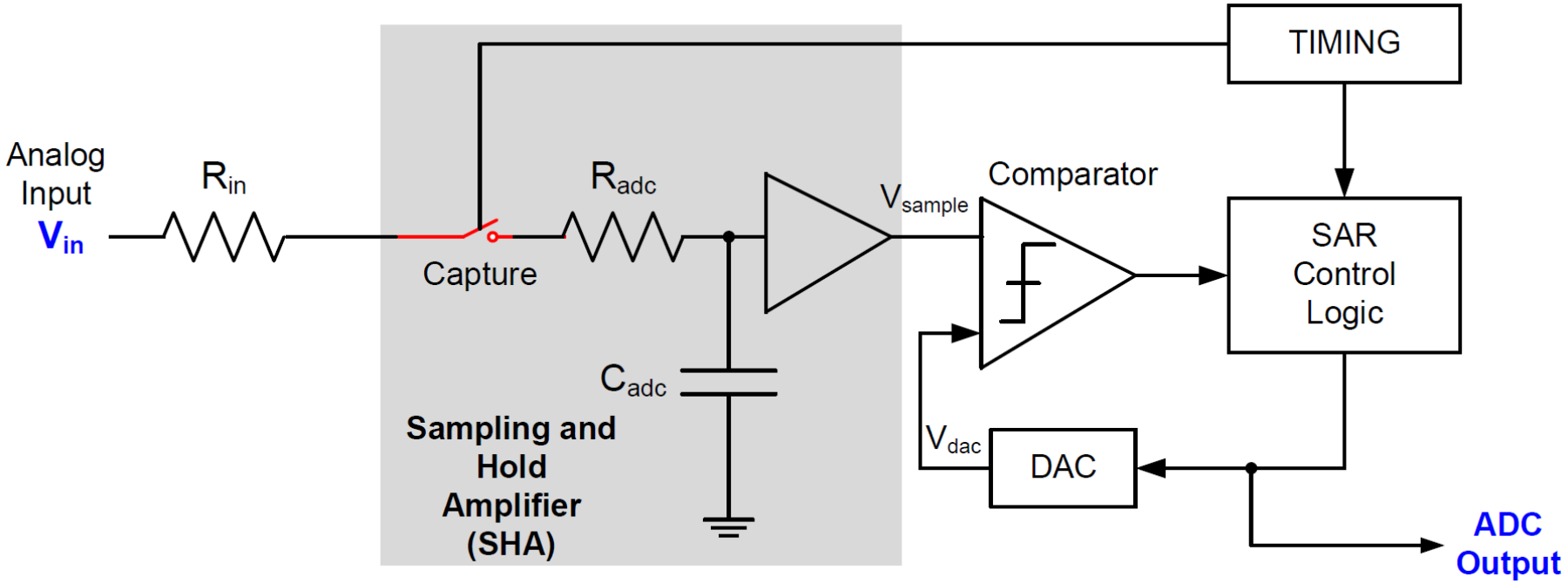


Popular ADC Architectures:

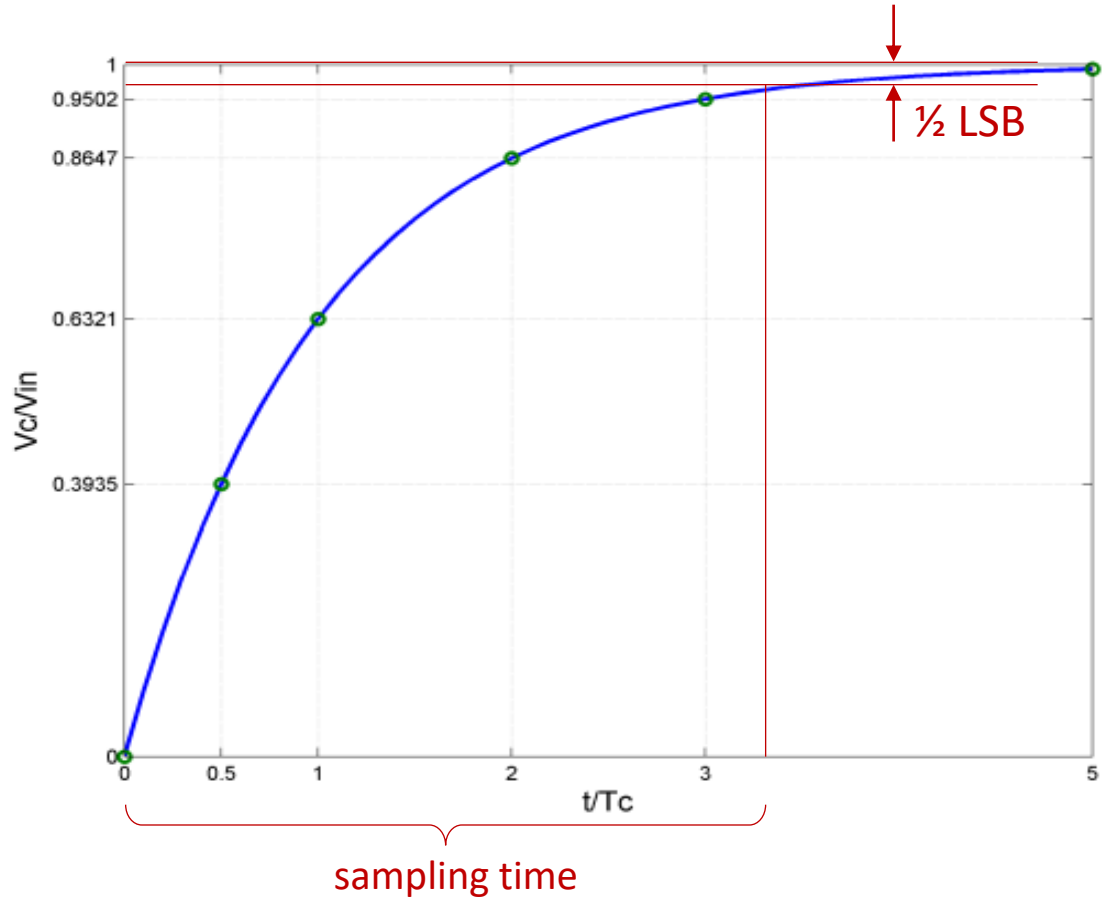
- Successive-approximation (SAR)
- Sigma-delta (Σ-Δ),
- Pipeline

https://www.analog.com/en/analog-dialogue/articles/the-right-adc-architecture.html

Successive-approximation (SAR)

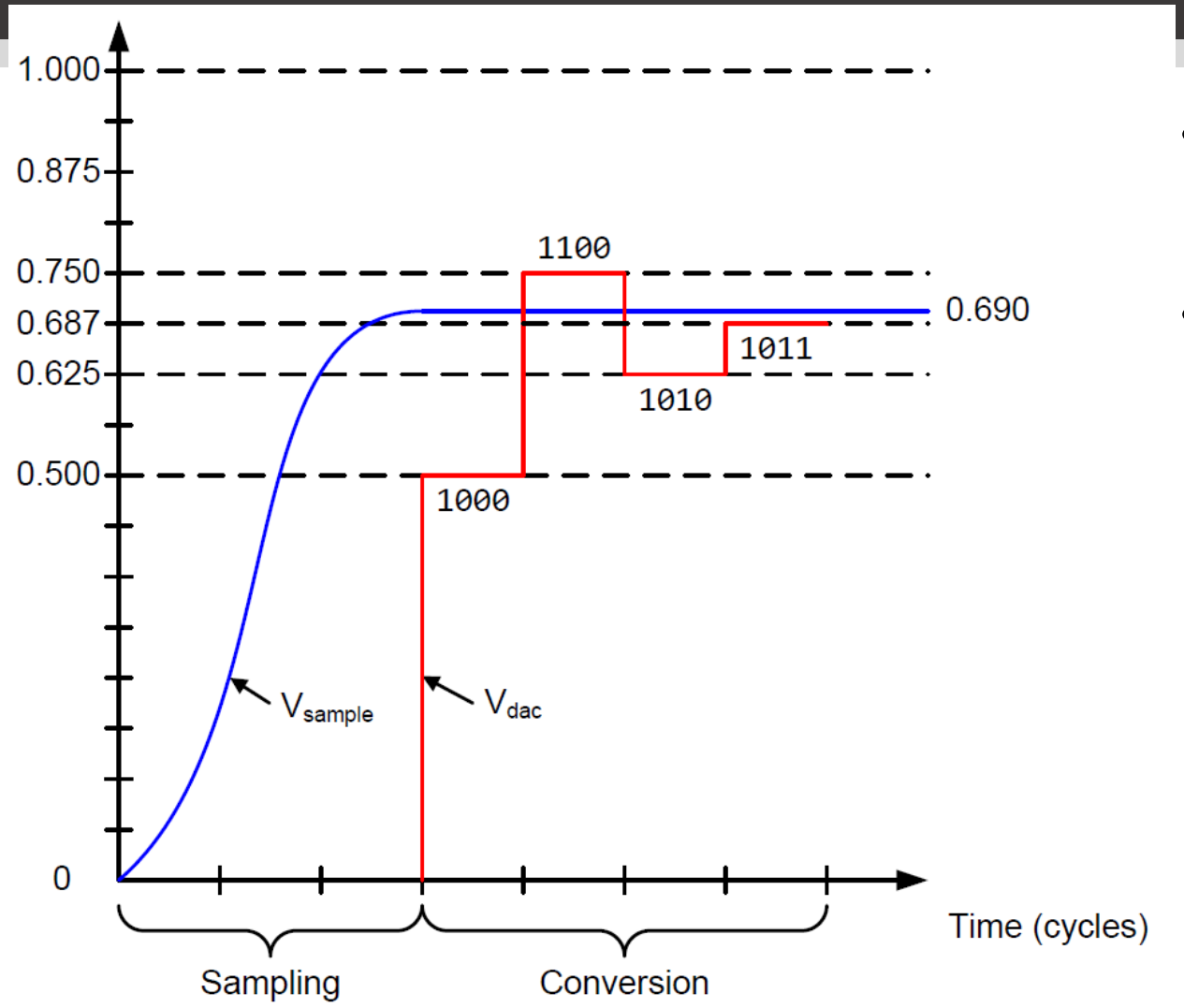


Determining Minimum Sampling Time



- Sampling time is software programmable
- Sampling time must large enough to settle within ½ LSB

Successive-approximation (SAR) ADC



N cycles for N-bit ADC

- Binary search algorithm to gradually approaches the input voltage
- Settle into ±½ LSB bound within the time allowed

ADC Conversion Time

$$T_{ADC} = T_{sampling} + T_{Conversion}$$

Suppose ADC clock = 16 MHz, and Sampling time = 4 cycles

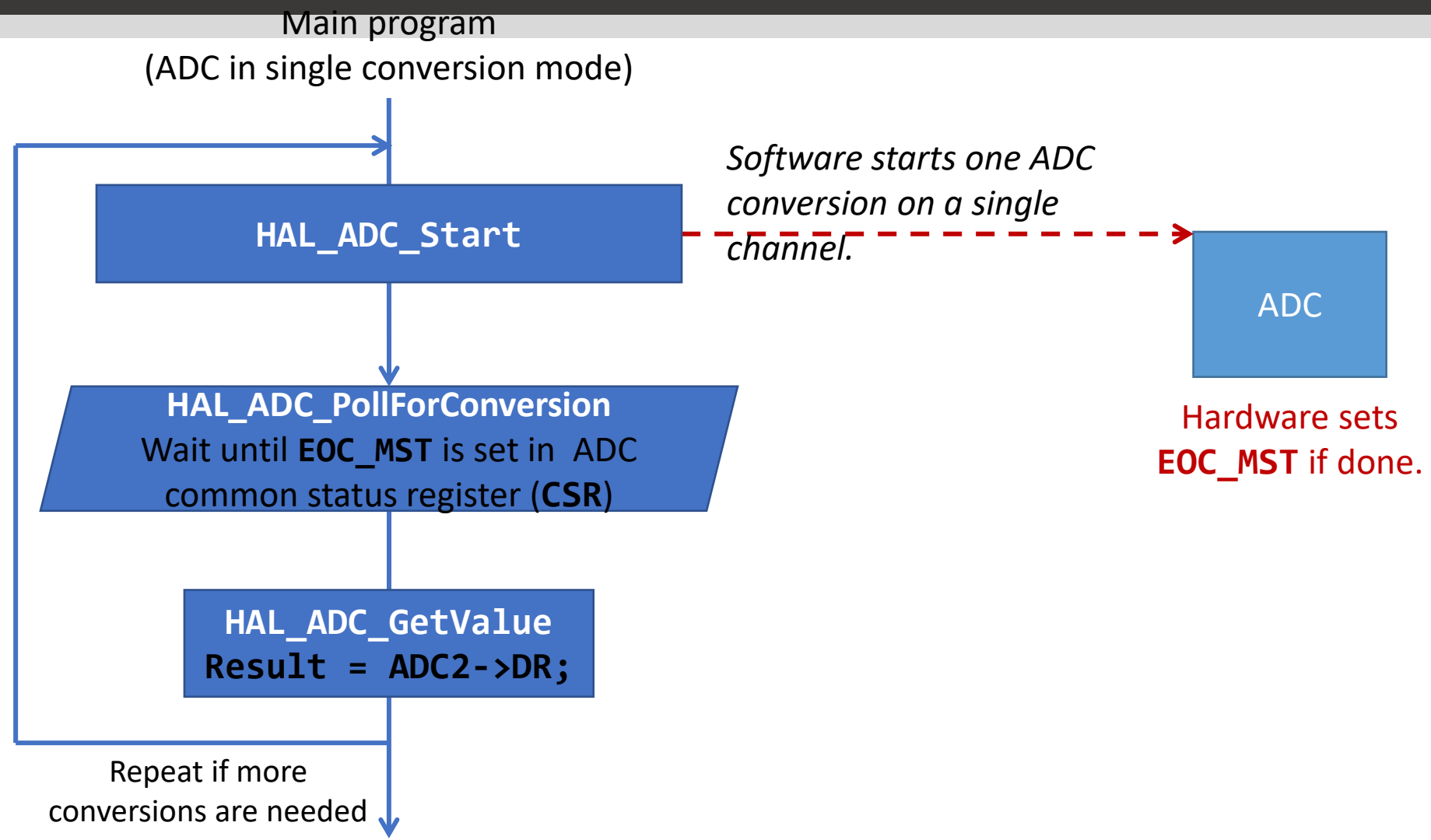
For 12-bit ADC

$$T_{ADC} = 4 + 12 = 16\ cycles = 1\ \mu s$$

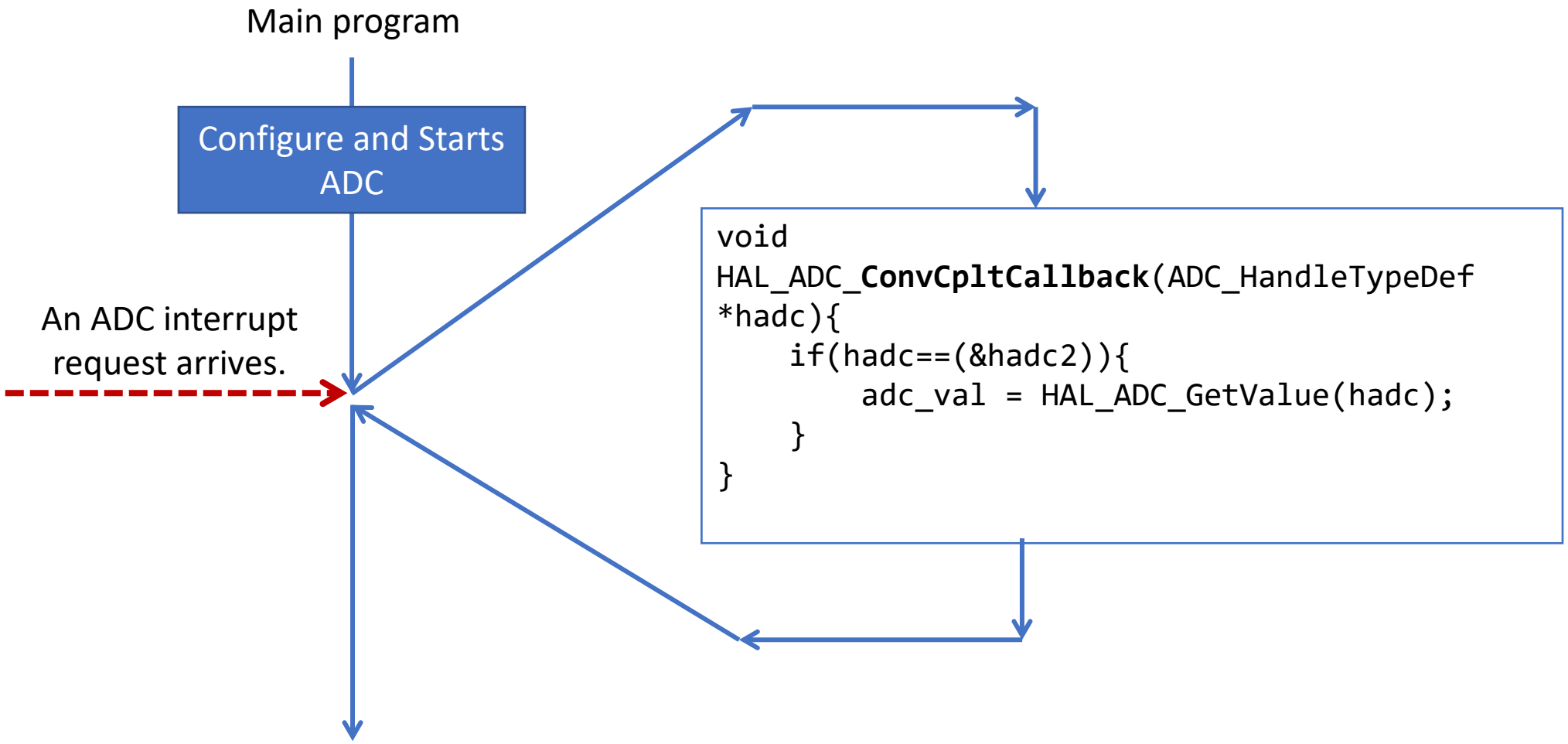
For 6-bit ADC

$$T_{ADC} = 4 + 6 = 10\ cycles = 0.625\ \mu s$$

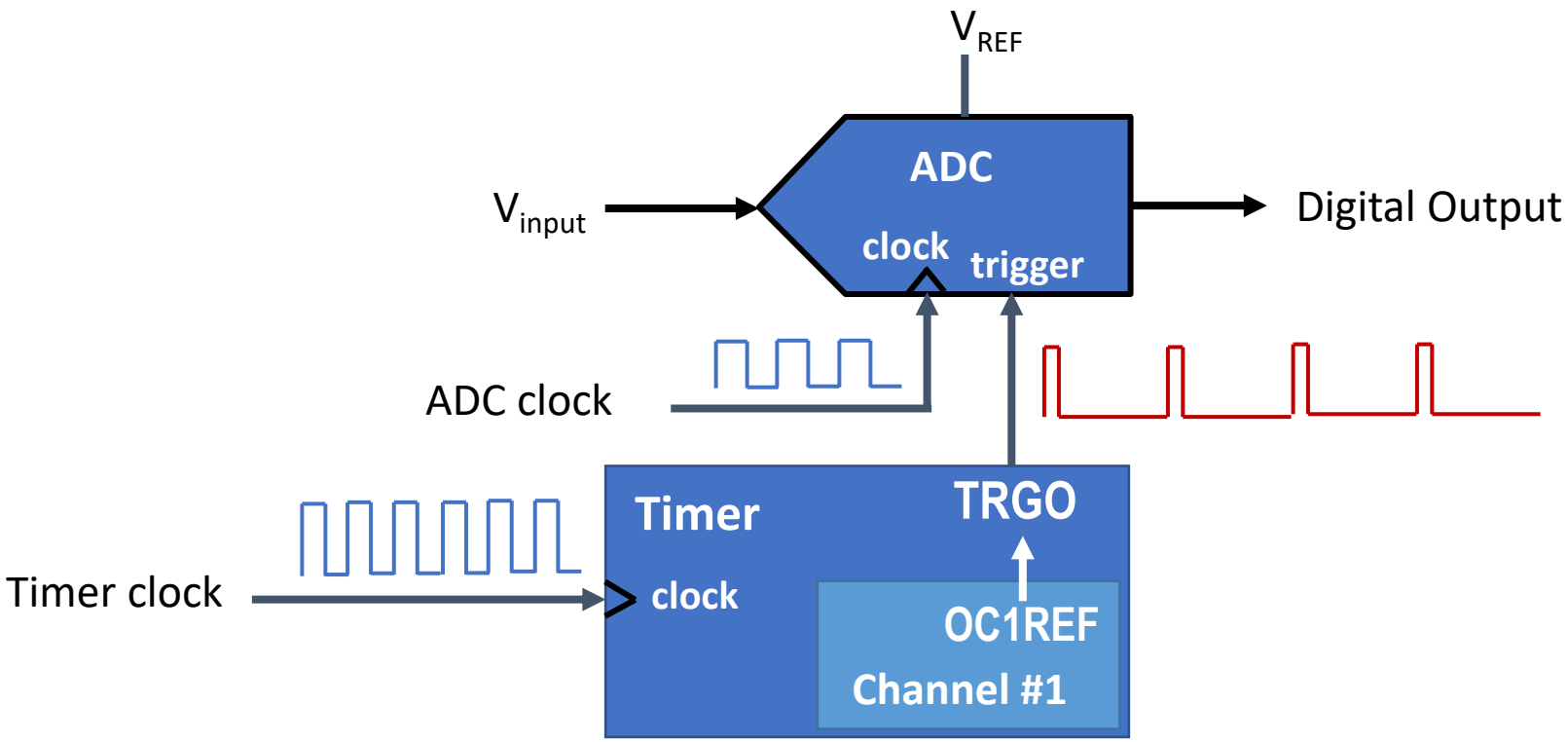
ADC with Polling (Busy Waiting)



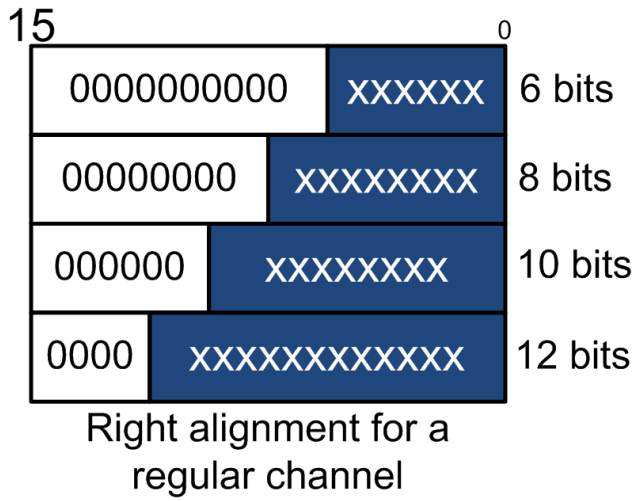
ADC with Interrupts



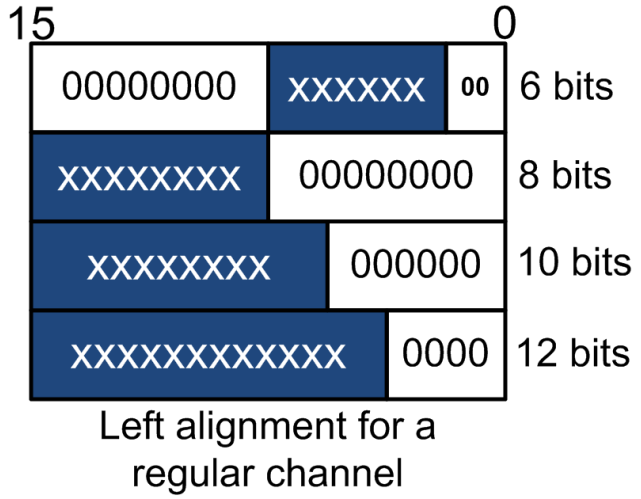
ADC Triggered by a Timer



Data Alignment



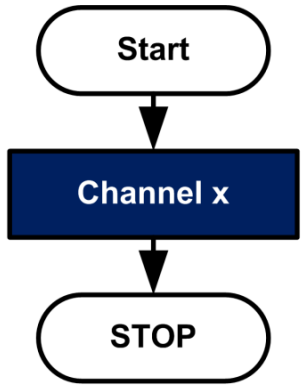
Right alignment for a regular channel



Left alignment for a regular channel

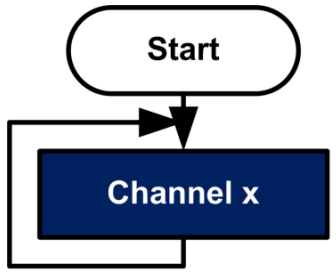
ADC Conversion Modes

Single Channel Mode



Single Channel, Single Conversion Mode

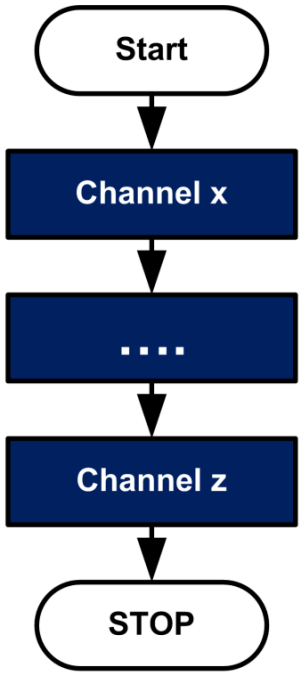
CONT in ADC_CR2 = 0
SCAN in ADC_CR2 = 0



Single Channel, Continuous Conversion Mode

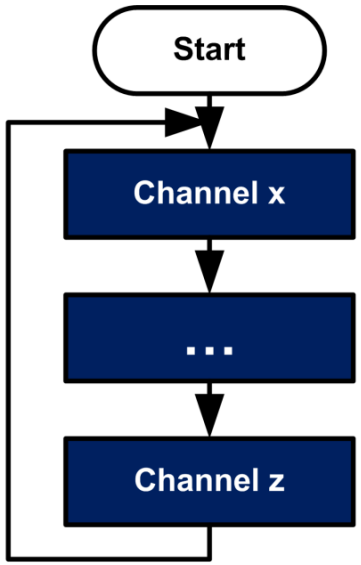
CONT in ADC_CR2 = 1
SCAN in ADC_CR2 = 0

Scan Mode



Scan Mode with Single Conversion

SCAN in ADC_CR2 = 1
CONT in ADC_CR2 = 0



Scan Mode with Continuous Conversion

SCAN in ADC_CR2 = 1
CONT in ADC_CR2 = 1

ADC: Regular *vs* injected