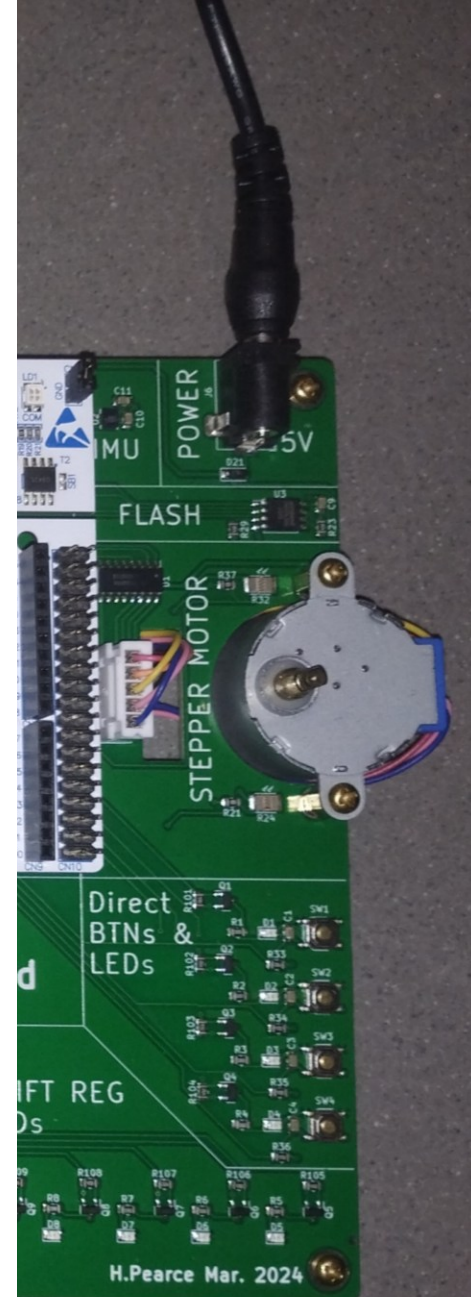


DESN2000
(Computer Engineering)
2026 T2

Analogue to Digital Converter

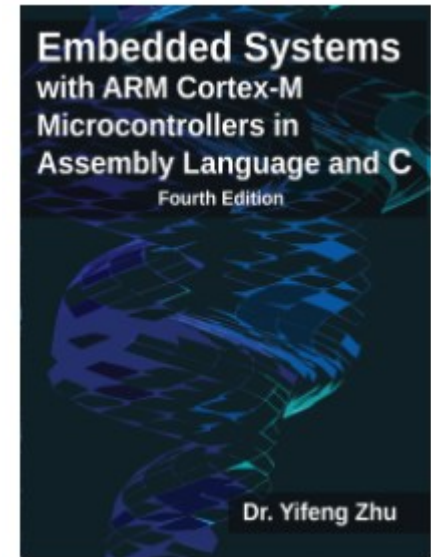
Hasindu Gamaarachchi



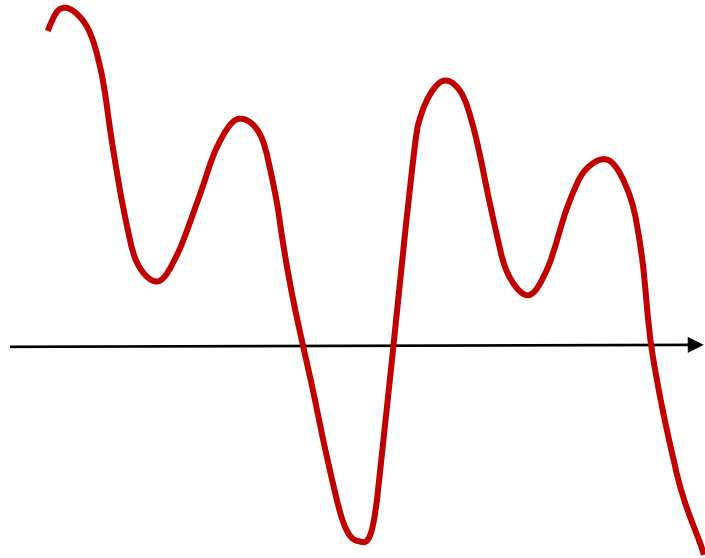
Learning Resources

The upcoming slides are adapted from “Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C (Fourth Edition)” – Yifeng Zhu

- Analog input and output - chapter 18

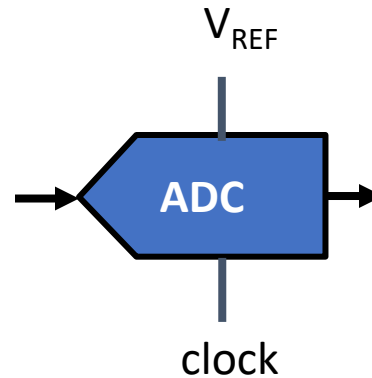


Analog-to-Digital Converter (ADC)

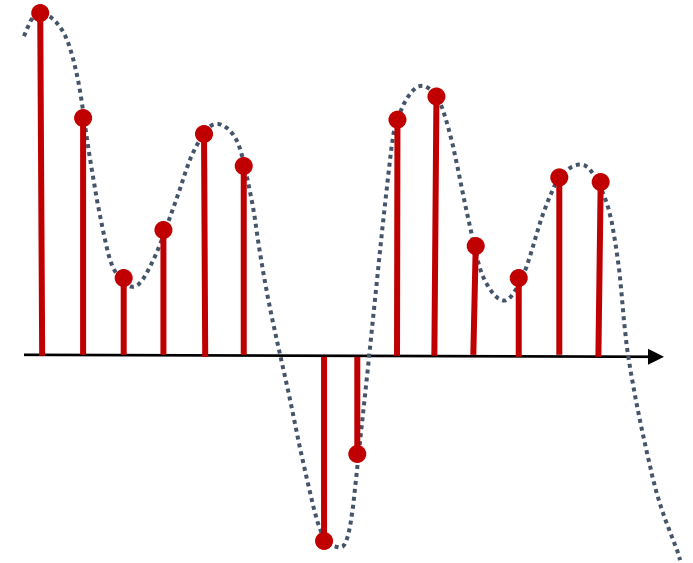


Analog signal $x(t)$

continuous time
continuous amplitude



- Resolution
- Quantization error
- Sampling rate

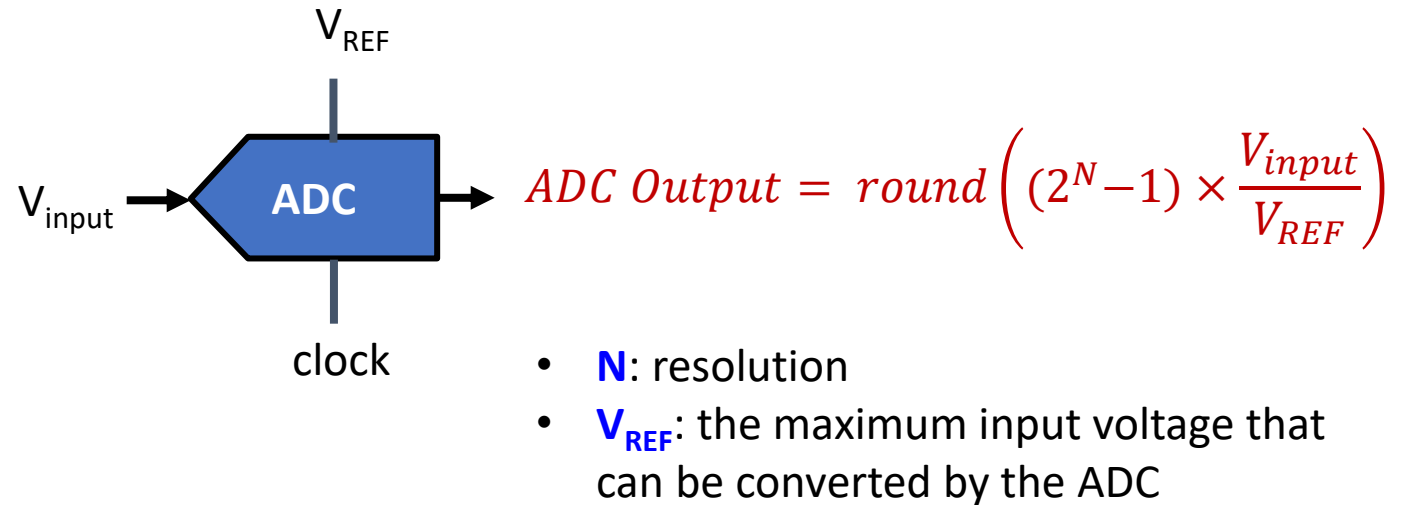


Digital values $x(n)$

discrete time
discrete amplitude

ADC: Resolution

- Resolution: number of binary bits in ADC output.



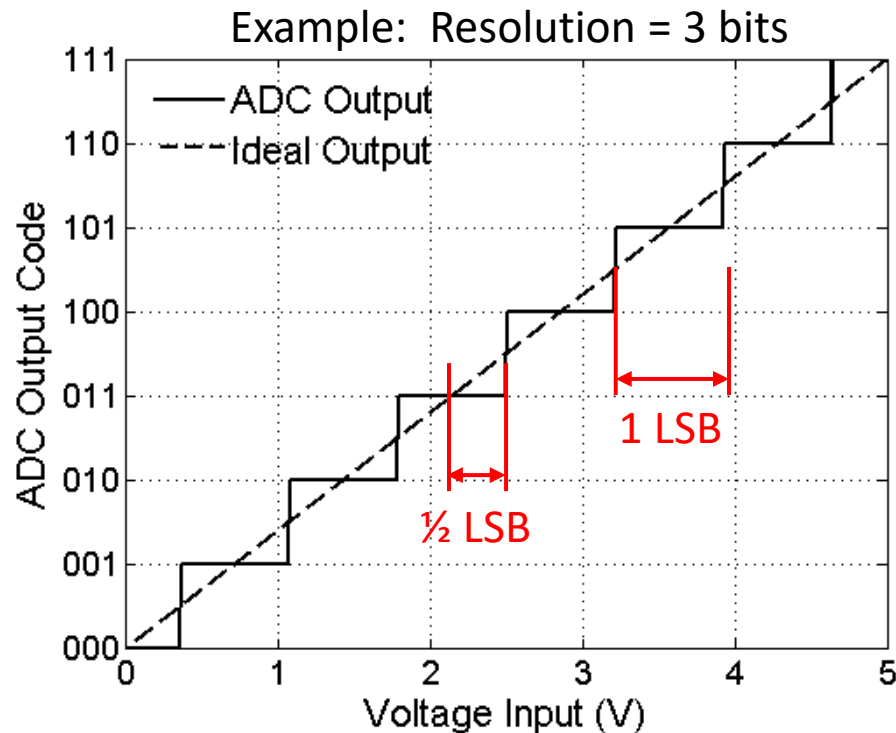
Example: for 10-bit ADC, $V_{input} = 1V$, $V_{REF} = 5V$

$$ADC\ Output = round\left(1023 \times \frac{1}{5}\right) = round(204.6) = 205 = 0xCD$$

ADC: Quantization Error

- Resolution N: number of binary bits in ADC output.

$$ADC\ Output = round\left((2^N - 1) \times \frac{V_{input}}{V_{REF}}\right)$$



Least significant bit (LSB) voltage

$$LSB = \frac{V_{REF}}{2^N - 1}$$

Max quantization error = $\pm \frac{1}{2}$ LSB

Example: 3-bit ADC and input range [0, 5V]

$$Max\ Quantization\ Error = \pm \frac{1}{2} LSB$$

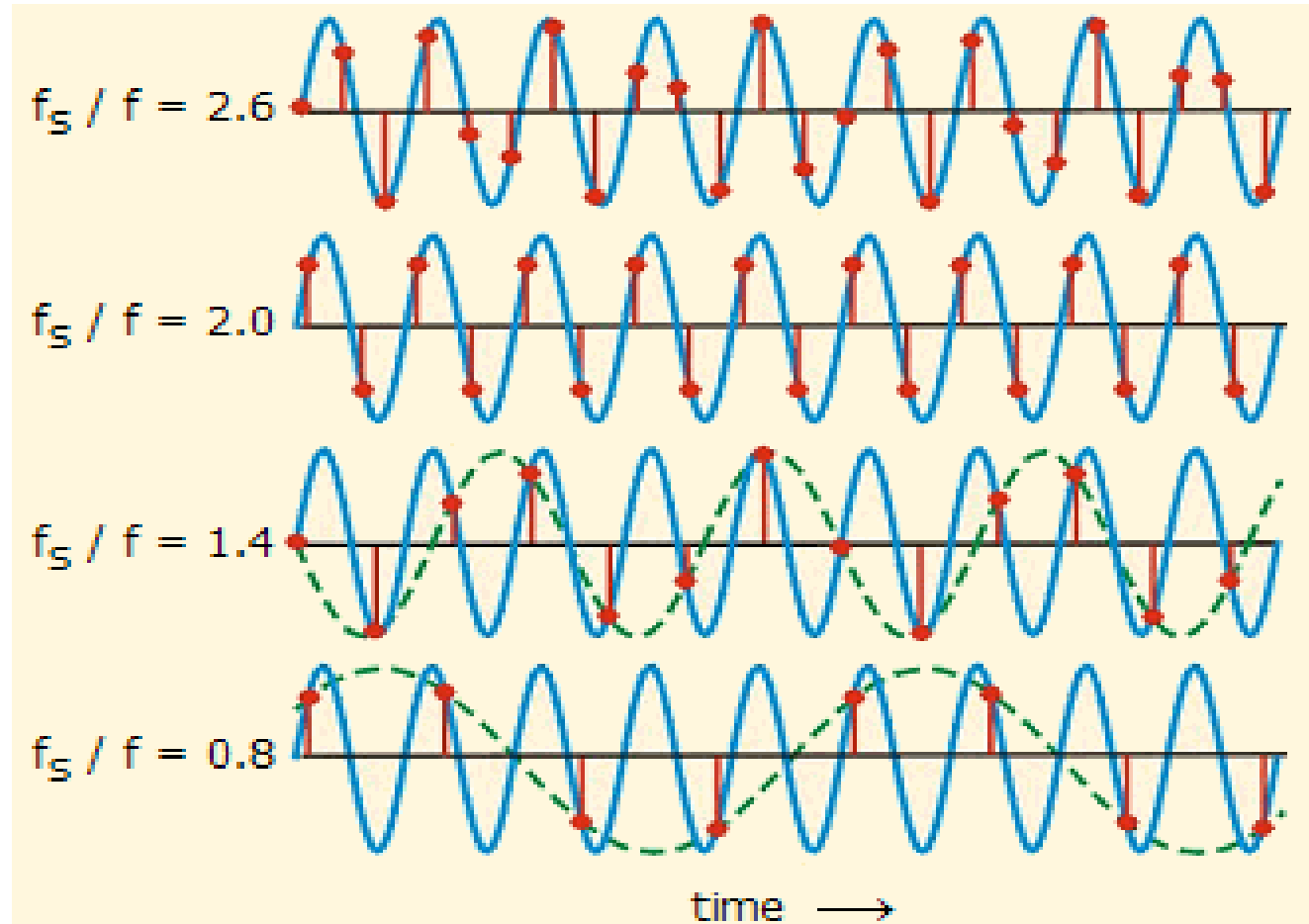
$$= \pm \frac{5V}{2 \times (2^3 - 1)}$$

$$= \pm 0.357\ V$$

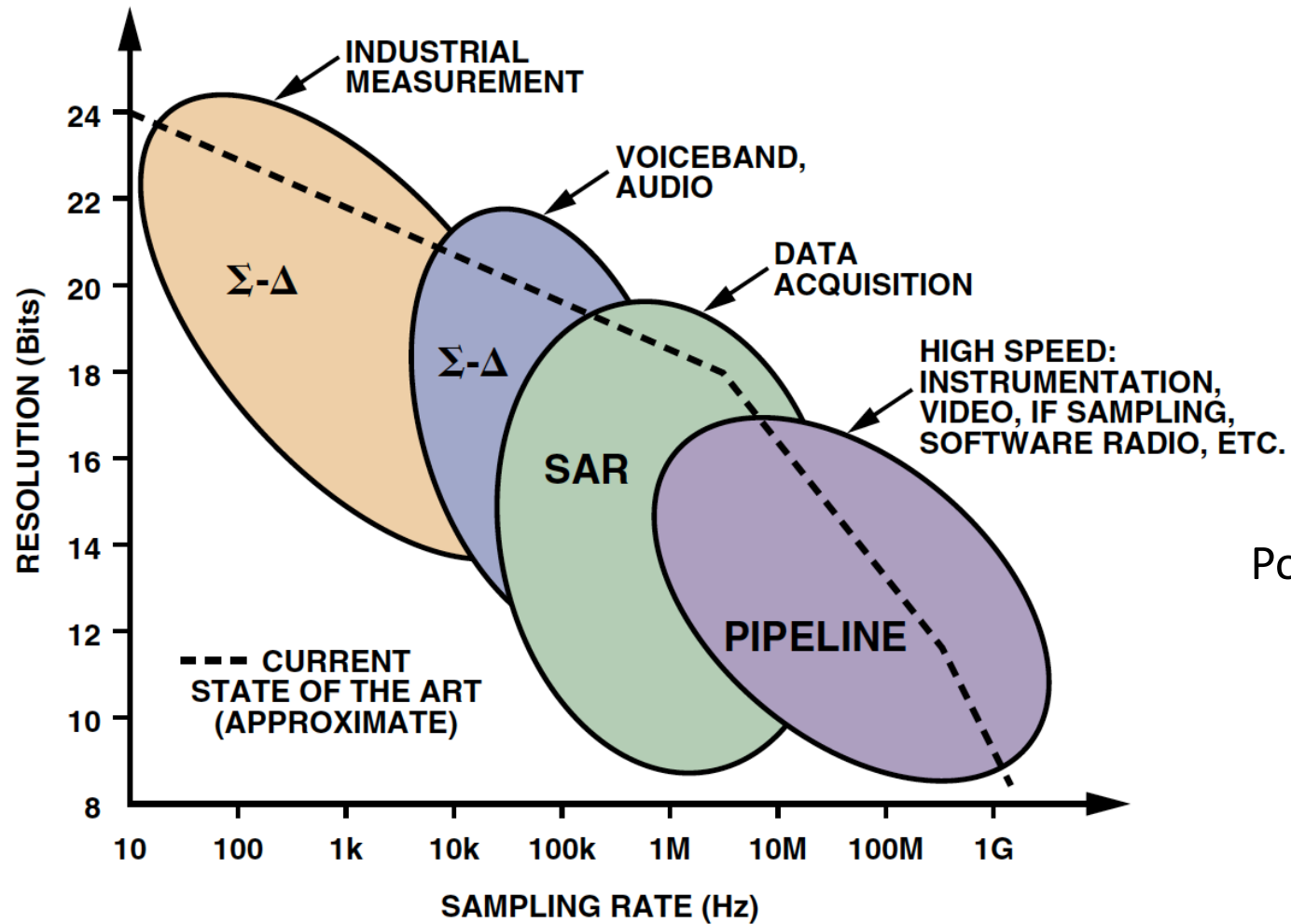
What sampling rate do we need?

Nyquist–Shannon Sampling Theorem

$$f_{\text{sampling}} \geq 2 \cdot f_{\text{signal}}$$



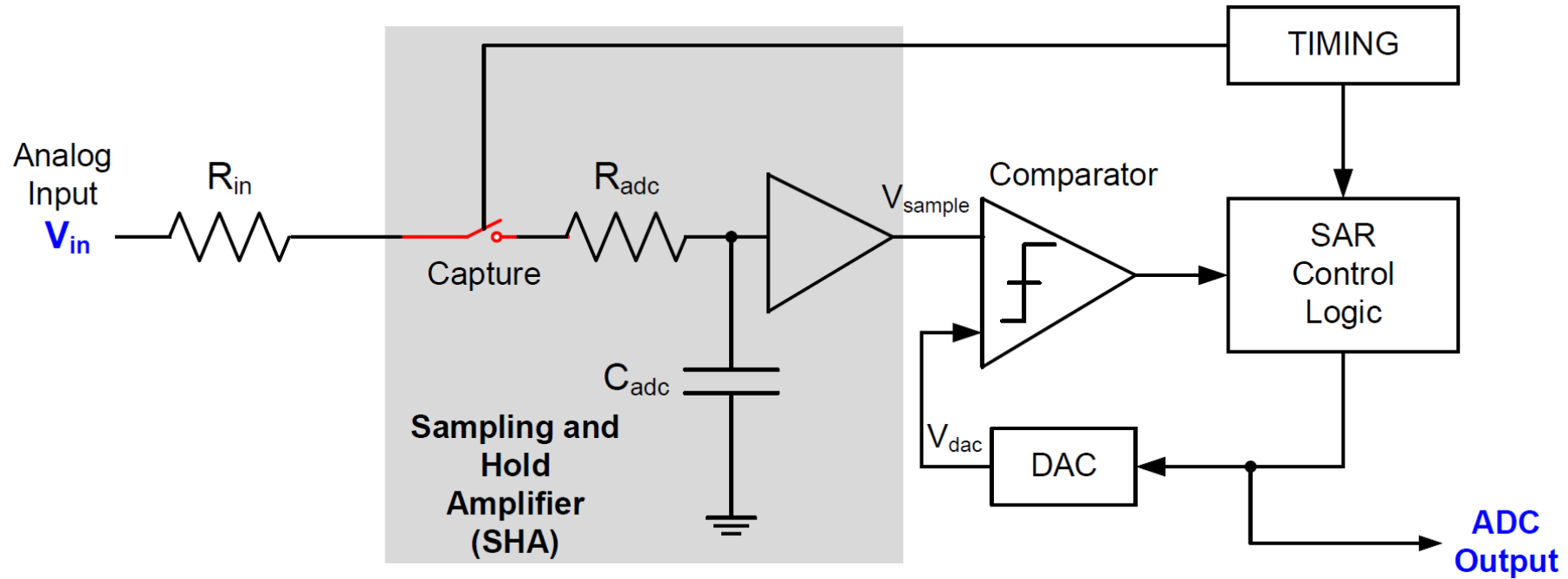
ADC Architecture



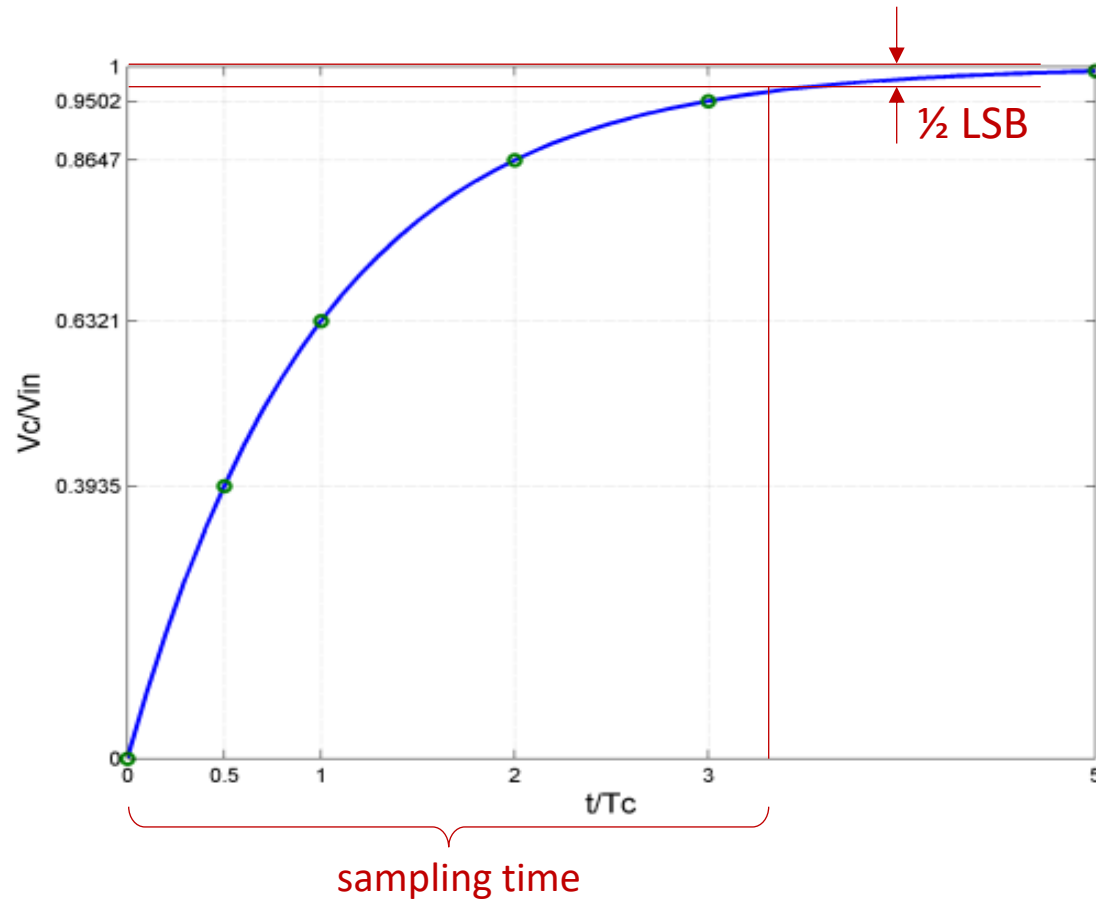
Popular ADC Architectures:

- Sigma-delta (Σ - Δ),
- Successive-approximation (SAR)
- Pipeline

Successive-approximation (SAR)

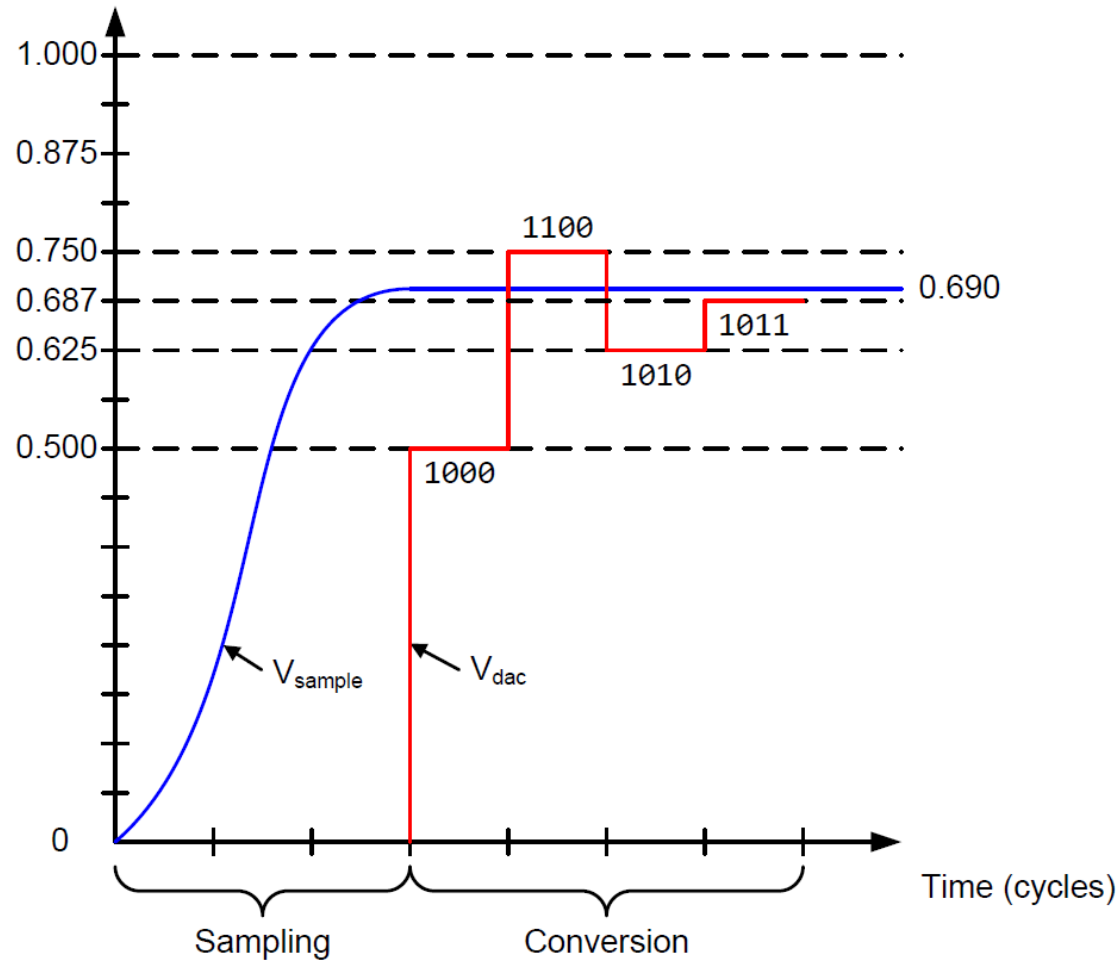


Determining Minimum Sampling Time



- Sampling time is software programmable
- Sampling time must large enough to settle within $\frac{1}{2}$ LSB

Successive-approximation (SAR) ADC



- **Binary search** algorithm to gradually approaches the input voltage
- Settle into $\pm 1/2$ LSB bound within the time allowed

N cycles for N-bit ADC

ADC Conversion Time

$$T_{ADC} = T_{sampling} + T_{Conversion}$$

Suppose ADC clock = 16 MHz, and Sampling time = 4 cycles

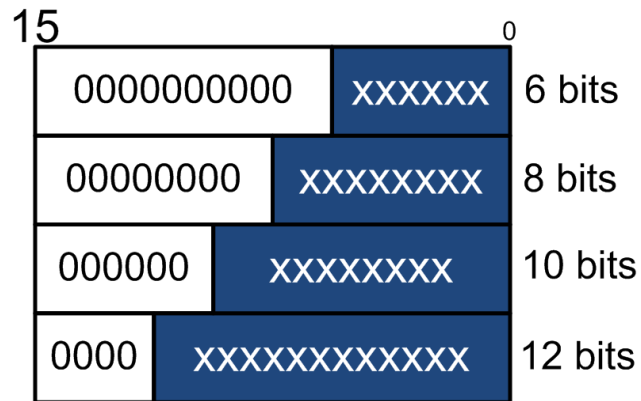
For 12-bit ADC

$$T_{ADC} = 4 + 12 = 16 \text{ cycles} = 1 \mu s$$

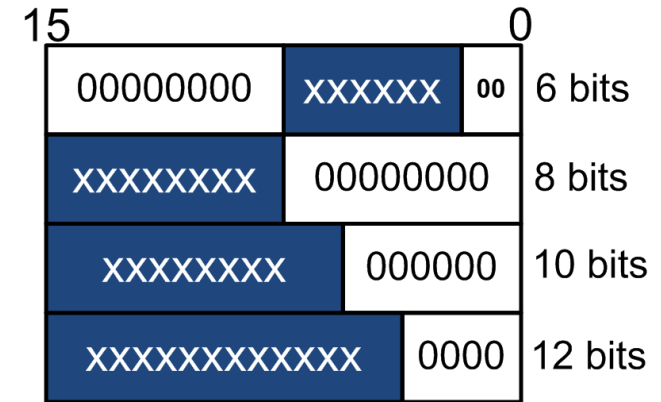
For 6-bit ADC

$$T_{ADC} = 4 + 6 = 10 \text{ cycles} = 0.625 \mu s$$

Data Alignment

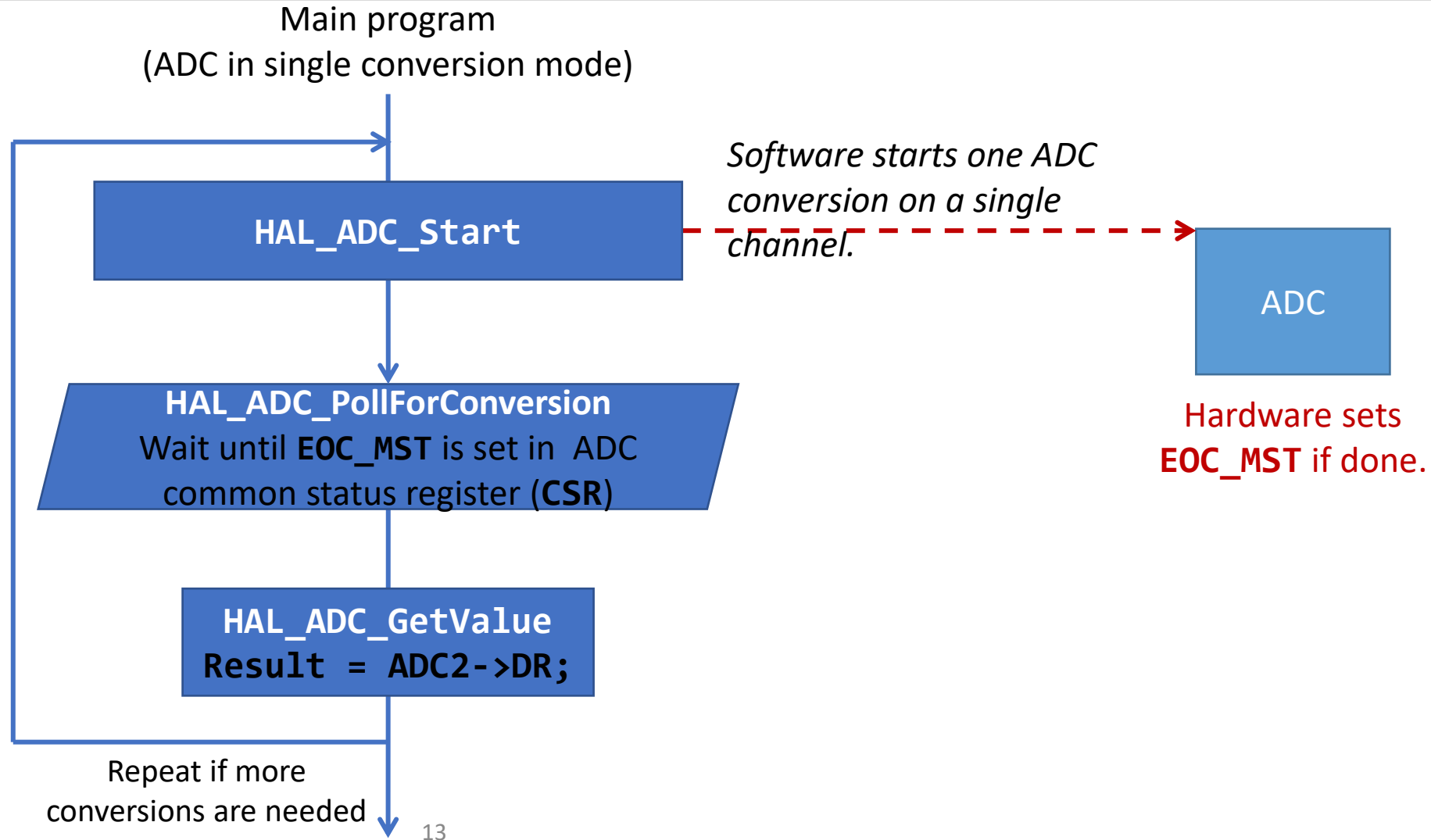


Right alignment for a regular channel

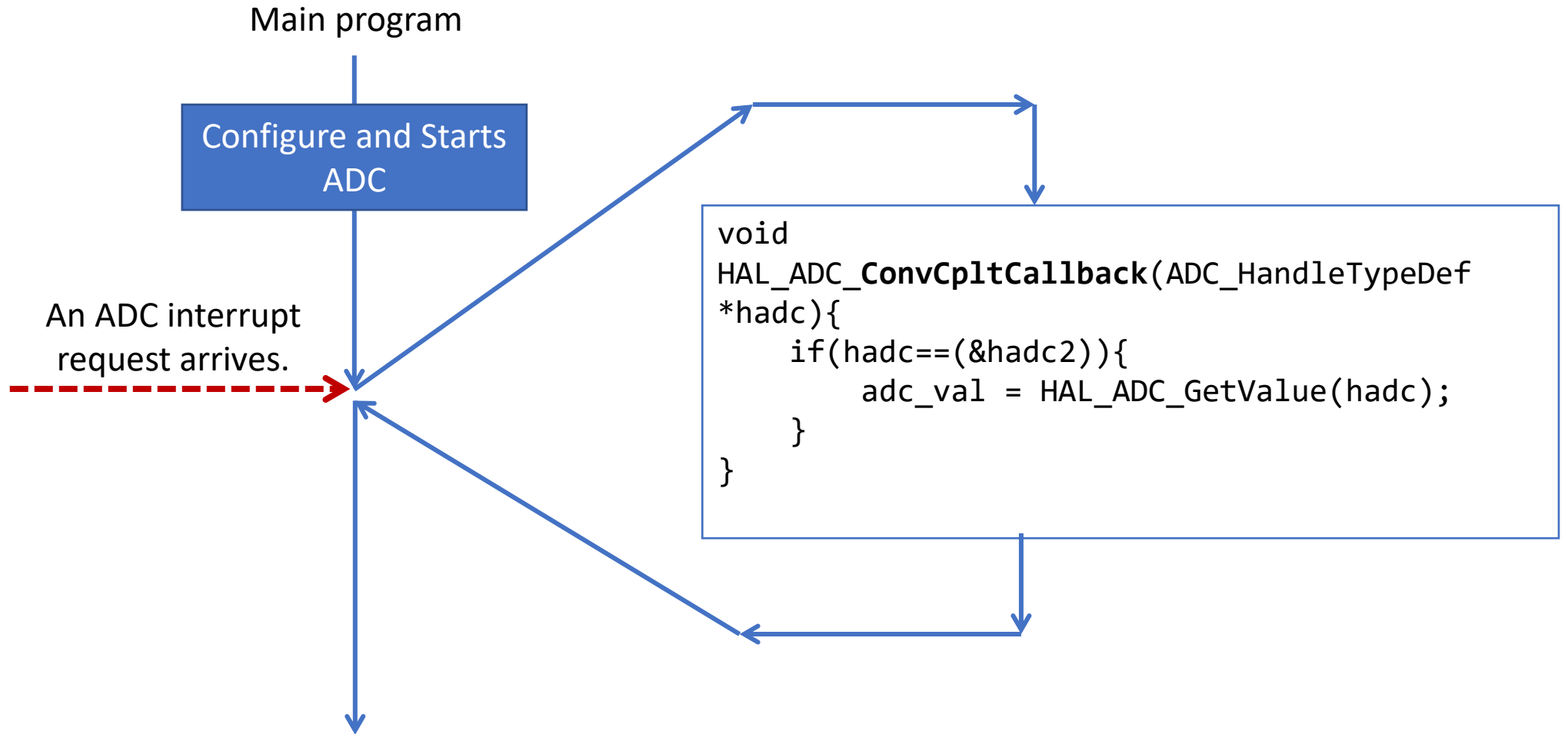


Left alignment for a regular channel

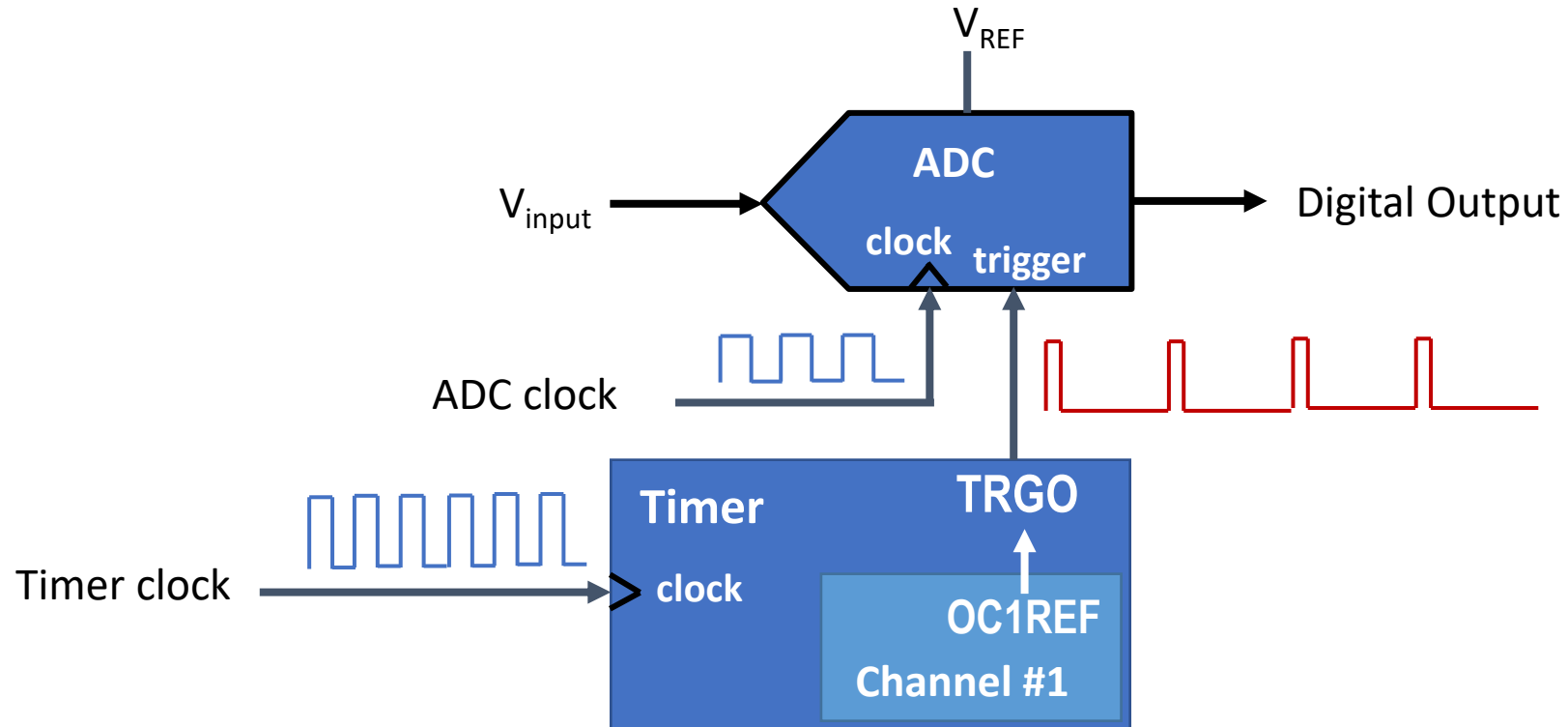
ADC with Polling (Busy Waiting)



ADC with Interrupts

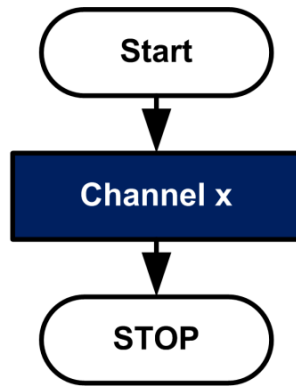


ADC Triggered by a Timer



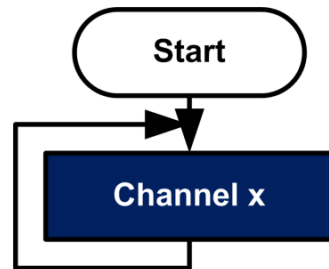
ADC Conversion Modes

Single Channel Mode



Single Channel, Single Conversion Mode

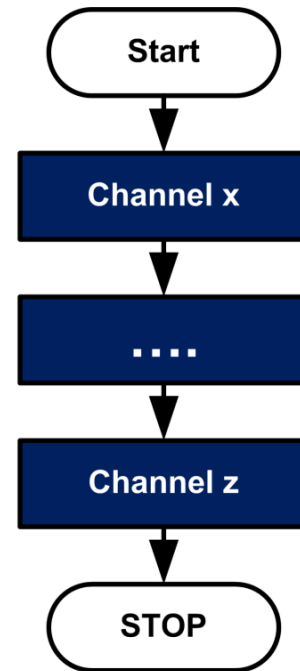
CONT in ADC_CR2 = 0
SCAN in ADC_CR2 = 0



Single Channel, Continuous Conversion Mode

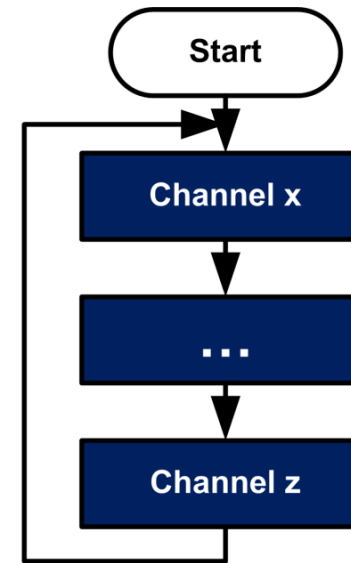
CONT in ADC_CR2 = 1
SCAN in ADC_CR2 = 0

Scan Mode



Scan Mode with Single Conversion

SCAN in ADC_CR2 = 1
CONT in ADC_CR2 = 0



Scan Mode with Continuous Conversion

SCAN in ADC_CR2 = 1
CONT in ADC_CR2 = 1

ADC: Regular vs injected

